ULTRA-LOW-VOLTAGE (ULV) IC DESIGN: DESIGNING FOR VDD BELOW kT/q

Outline

1 The MOSFET : DC and small signal models

2 ULV CMOS logic circuits

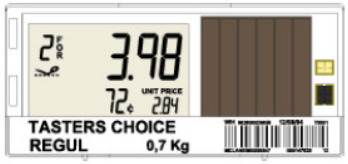
3 ULV rectifiers

4 ULV oscillators

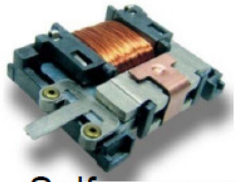
Self-powered applications

Low data rate, low duty cycle, ultra-low power

Solar Keyboard

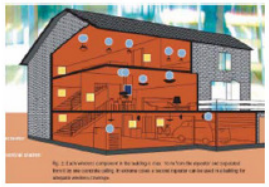


Electronic Shelf Labels

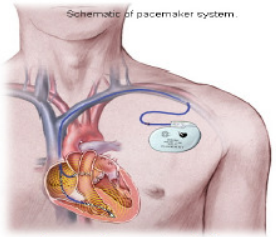


Self-powered switches

Convenience



Occupancy Sensor



Implantables

Pipelines

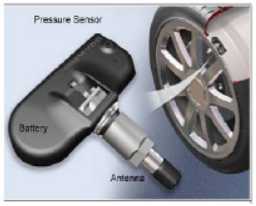
Oil Rig

Environmental Awareness

Smoke Detector

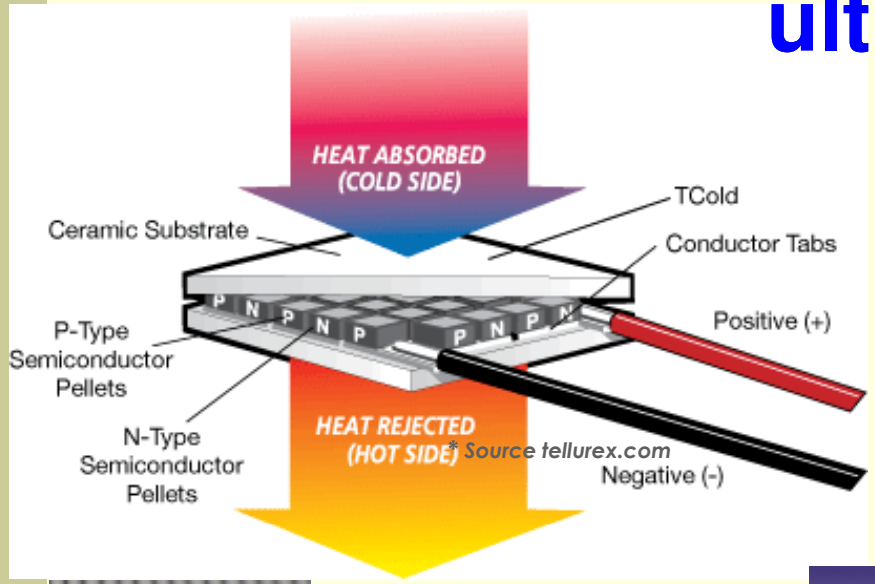
Structural sensors

Hard to Reach

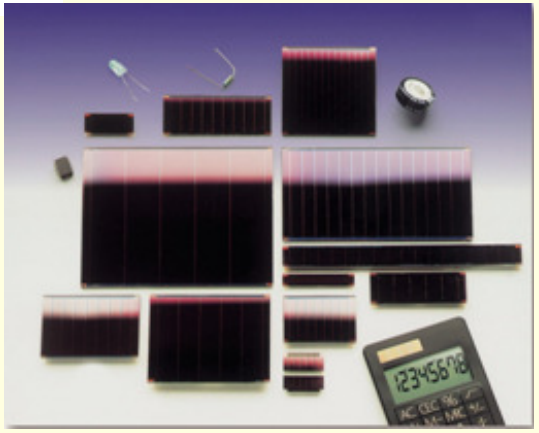


TPMS

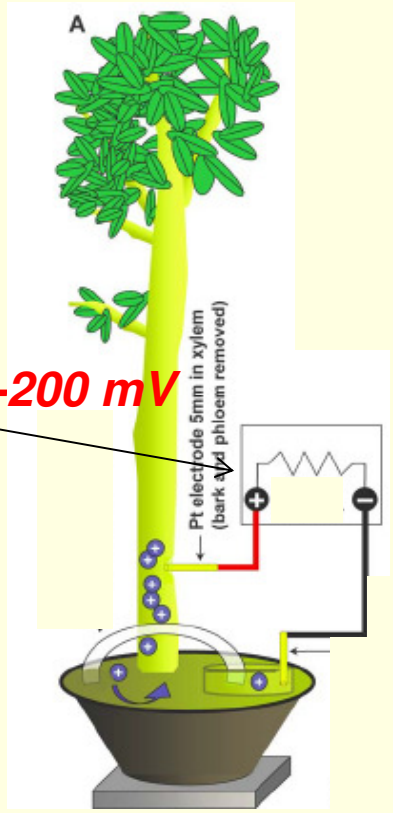
Ambient DC power supply voltages are ultra low



Vo ≅ ***50 mV***



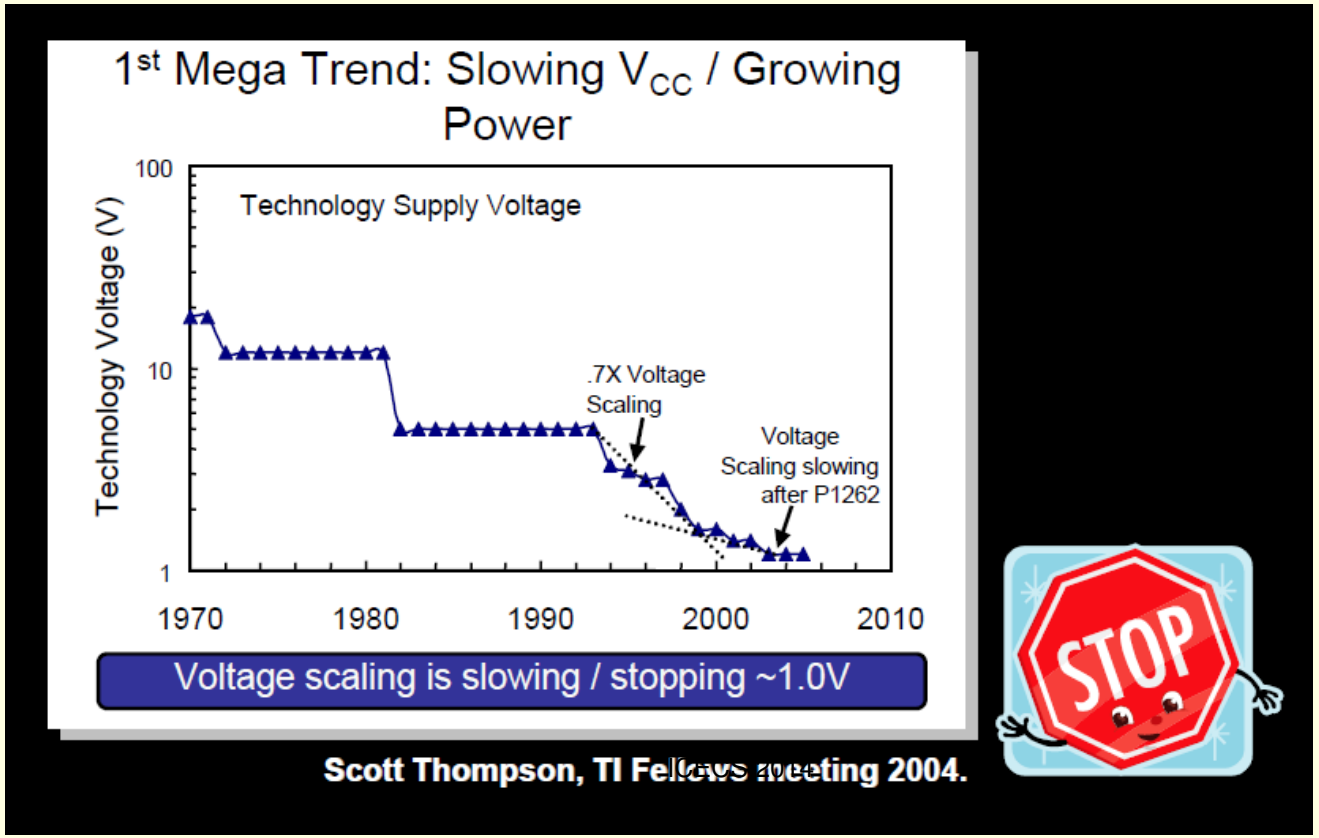
Vo $_{(interiors)}$ ≅ ***100 mV***



Vo ≅ ***20-200 mV***

The trend toward low supply voltages

- Q1-Are there lower bounds on the supply voltages to power electronic circuits?
- Q2-What are the best technologies for ultra low voltage circuits?



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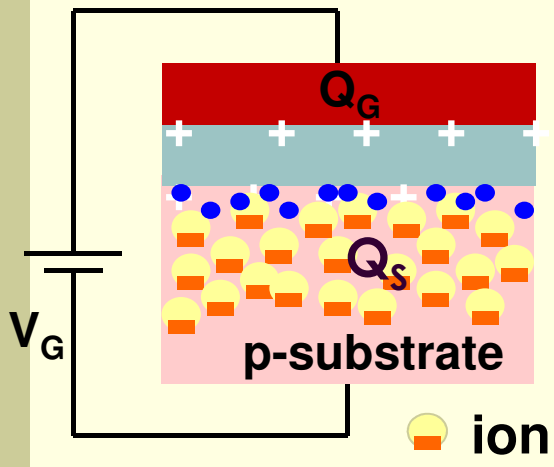
ULTRA-LOW-VOLTAGE (ULV) IC DESIGN: DESIGNING FOR VDD BELOW kT/q

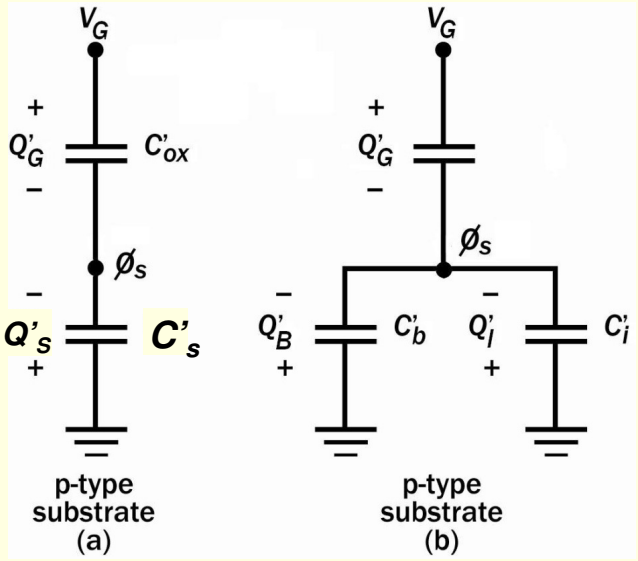
Chapter 1

The MOSFET : DC and small signal models

MOSFET capacitive model in inversion



Many electrons approach the surface!



$$C'_{gb} = \frac{dQ'_G}{dV_G}$$

$$C'_{gb} = \frac{1}{\frac{1}{C'_s} + \frac{1}{C'_{ox}}}$$

$$C'_s = -\frac{dQ'_S}{d\phi_s} = -\frac{d\left(Q'_B + Q'_I\right)}{d\phi_s} = C'_b + C'_i$$

ϕ_S - surface potential

C'_{ox} - oxide capacitance/unit area

Q'_G (Q'_S) - gate (semiconductor) charge/ unit area

Q'_I (Q'_B) - inversion (depletion) charge/unit area

C'_i (C'_b) - inversion (depletion) capacitance /unit area

Main approximation for compact MOS modeling: the charge-sheet model

Minority carriers occupy a *zero-thickness* layer at the Si-SiO_2 interface, where $\phi = \phi_s$

$$Q_I' \propto e^{\phi_s/\phi_t} \Rightarrow C_i' = -\frac{dQ_I'}{d\phi_s} = -\frac{Q_I'}{\phi_t}$$

Charge-sheet + depletion approximation for the bulk charge gives

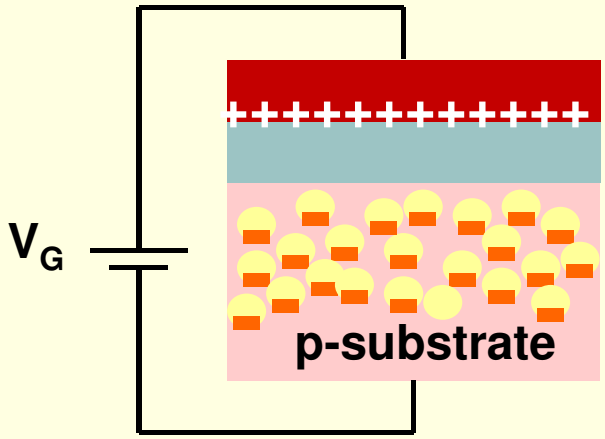
$$Q_B' \cong -qN_A x_d = -\sqrt{2q\varepsilon_s N_A \phi_s}$$

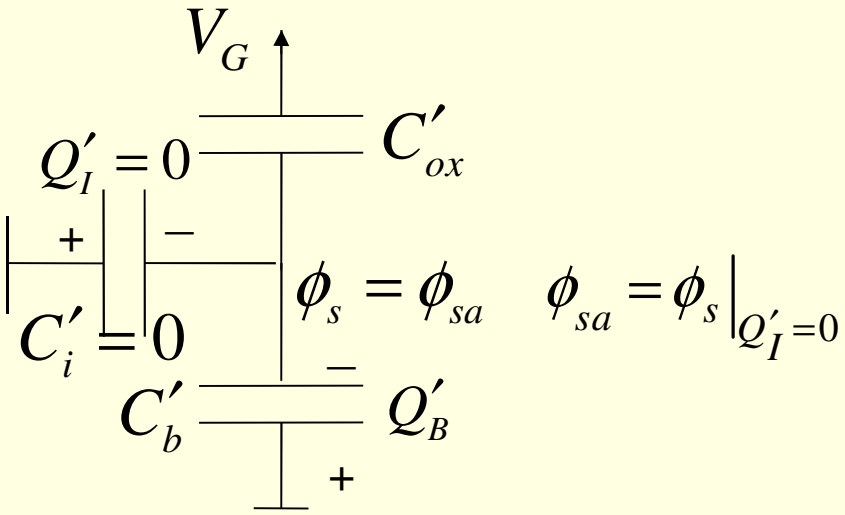
$$C_b' \cong \frac{\sqrt{2q\varepsilon_s N_A}}{2\sqrt{\phi_s}} = \frac{\gamma C_{ox}'}{2\sqrt{\phi_s}}$$

$$\gamma = \sqrt{2q\varepsilon_s N_A}/C_{ox}'$$

is the body-effect coefficient

Surface potential for negligible inversion charge : ϕ_{sa}



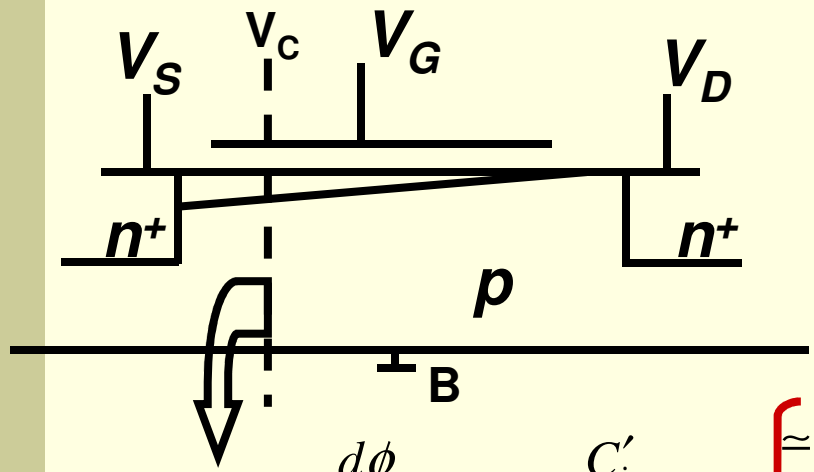


Threshold voltage $V_G = V_{T0} \leftrightarrow \phi_s \cong 2\phi_F$ $\quad \dfrac{\Delta\phi_{sa}}{\Delta V_G} \cong \dfrac{C'_{ox}}{C'_{ox} + C'_b} = \dfrac{1}{n}$

$$\phi_{sa} \cong 2\phi_F + \frac{V_G - V_{T0}}{n} = 2\phi_F + V_P$$

V_P is the pinch-off voltage

Unified Charge Control Model-1



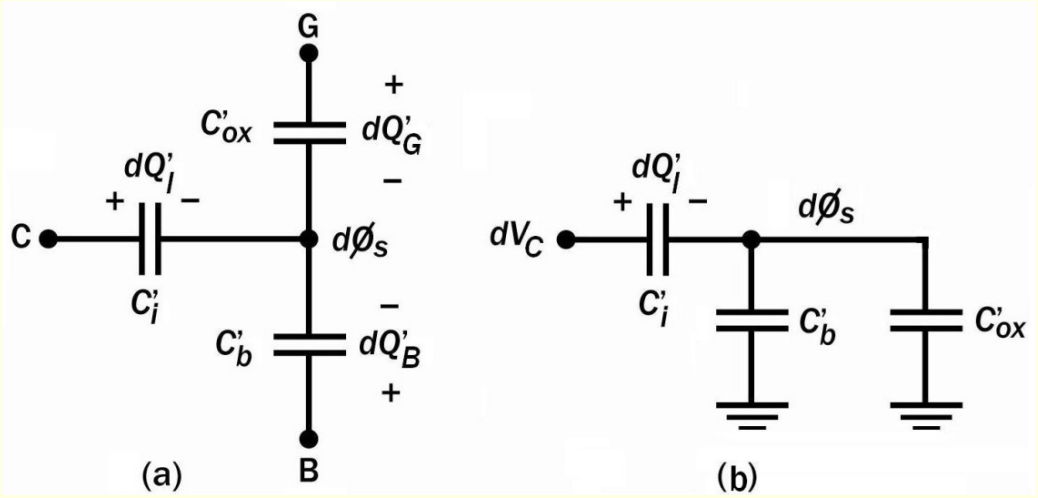
$$C'_{ox} + C'_b = nC'_{ox}$$

$$n = n(V_G)$$

$$dQ'_I = nC'_{ox}\,d\phi_s$$

$$\frac{d\phi_s}{dV_C} = \frac{C'_i}{C'_i + C'_{ox} + C'_b} \begin{cases} \simeq -\dfrac{Q'_I}{nC'_{ox}\phi_t} < 1 & \text{WI} \\ \simeq 1 & \text{SI} \end{cases}$$

$$C'_i = -\frac{Q'_I}{\phi_t}$$



$$dV_C = dQ'_I\left(\frac{1}{nC'_{ox}} - \frac{\phi_t}{Q'_I}\right)$$

$$V_S \le V_C \le V_D$$

Unified Charge Control Model (UCCM) -2

$$dQ_I'\left(\frac{1}{nC_{ox}'}-\frac{\phi_t}{Q_I'}\right)=dV_C$$

Integrating from an arbitrary channel potential V_C to a reference potential V_P yields UCCM

$$n=1+\frac{C_b'}{C_{ox}'}=n\left(V_G\right)$$

$$Q_{IP}'=Q_I'\big|_{V_C=V_P}$$

$$V_P-V_C=\phi_t\left[\frac{Q_{IP}'-Q_I'}{nC_{ox}'\phi_t}+\ln\left(\frac{Q_I'}{Q_{IP}'}\right)\right]$$

Choosing the thermal charge as the pinch-off charge

$$Q_{IP}'=-nC_{ox}'\phi_t$$

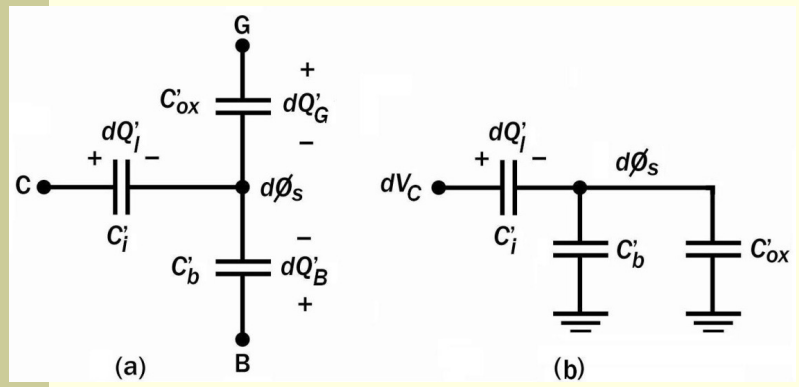
The normalized inversion (areal) charge density is

$$\frac{Q_I'}{Q_{IP}'}=q_I'$$

Normalized UCCM

$$V_P-V_C=\phi_t\left(q_I'-1+\ln q_I'\right)$$

Charge control current model



$$I_D = -\mu_n W Q_I' \frac{d\phi_s}{dy} + \mu_n W \phi_t \frac{dQ_I'}{dy}$$

$$dQ_I' = (C_{ox}' + C_b')d\phi_s = nC_{ox}' d\phi_s$$

***n=n*(V_G) is constant along the channel**

$$I_D = -\frac{\mu_n W}{nC_{ox}'}(Q_I' - \phi_t n C_{ox}')\frac{dQ_I'}{dy}$$

Integrating along the channel yields

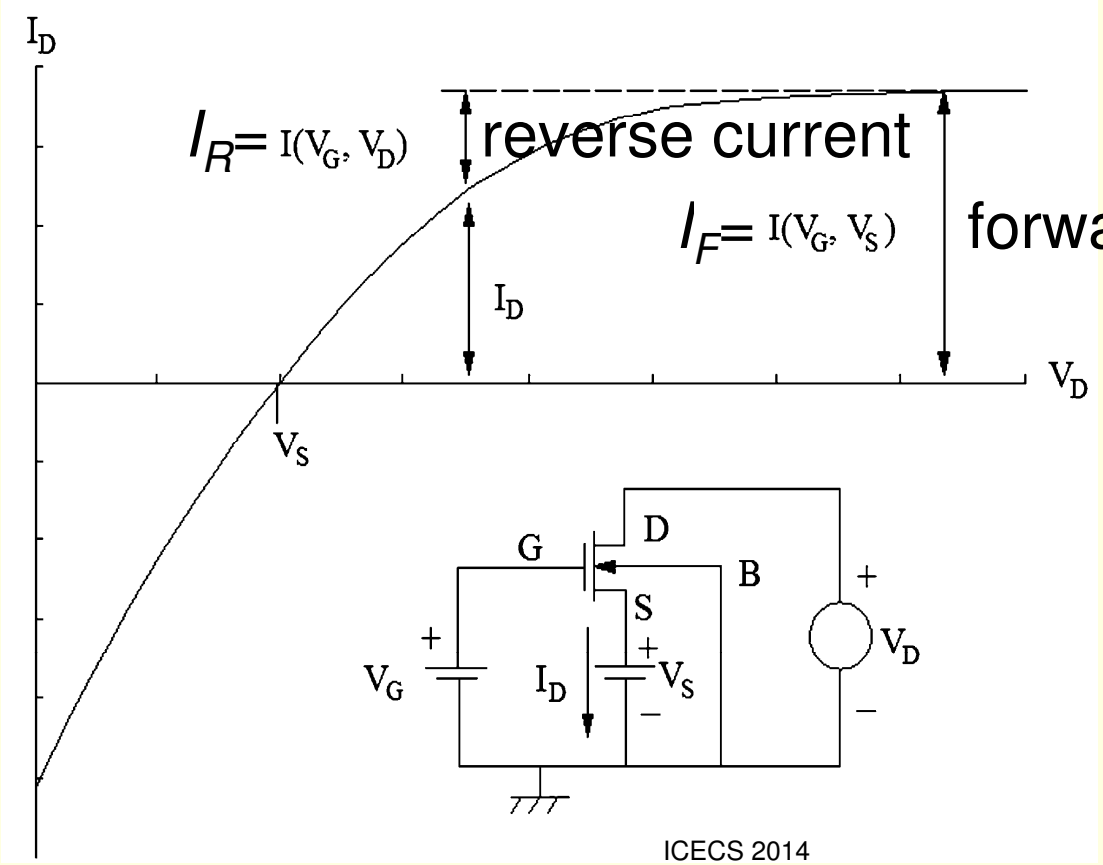
$$I_D = \frac{\mu_n W}{L}\left[\frac{Q_{IS}'^{\,2} - Q_{ID}'^{\,2}}{2nC_{ox}'} - \phi_t\left(Q_{IS}' - Q_{ID}'\right)\right]$$

Forward and reverse currents

symmetry of the rectangular MOSFET

$$I_D = I_F - I_R = I(V_G, V_S) - I(V_G, V_D)$$

$$I_{F(R)} = \frac{W}{L}\mu_n \left[\frac{Q'^2_{IS(D)}}{2nC'_{ox}} - \phi_t Q'_{IS(D)} \right]$$



Normalization (areal) charge

$$I_D = -\frac{\mu_n W}{nC'_{ox}}(Q'_I - \phi_t nC'_{ox})\frac{dQ'_I}{dy}$$

Drift Diffusion

$$Q'_I = -nC'_{ox}\phi_t$$

Drift = Diffusion

Normalization charge

$$q'_{IS(D)} = Q'_{IS(D)} / \left(-nC'_{ox}\phi_t\right)$$

$$I_D = I_F - I_R = I_S\left[i_f - i_r\right]$$

Normalized unified charge control model

$$V_P - V_C = \phi_t\left(q'_I - 1 + \ln q'_I\right)$$

$$i_{f(r)} = I_{F(R)} / I_S = \left(1 + q'_{IS(D)}\right)^2 - 1$$

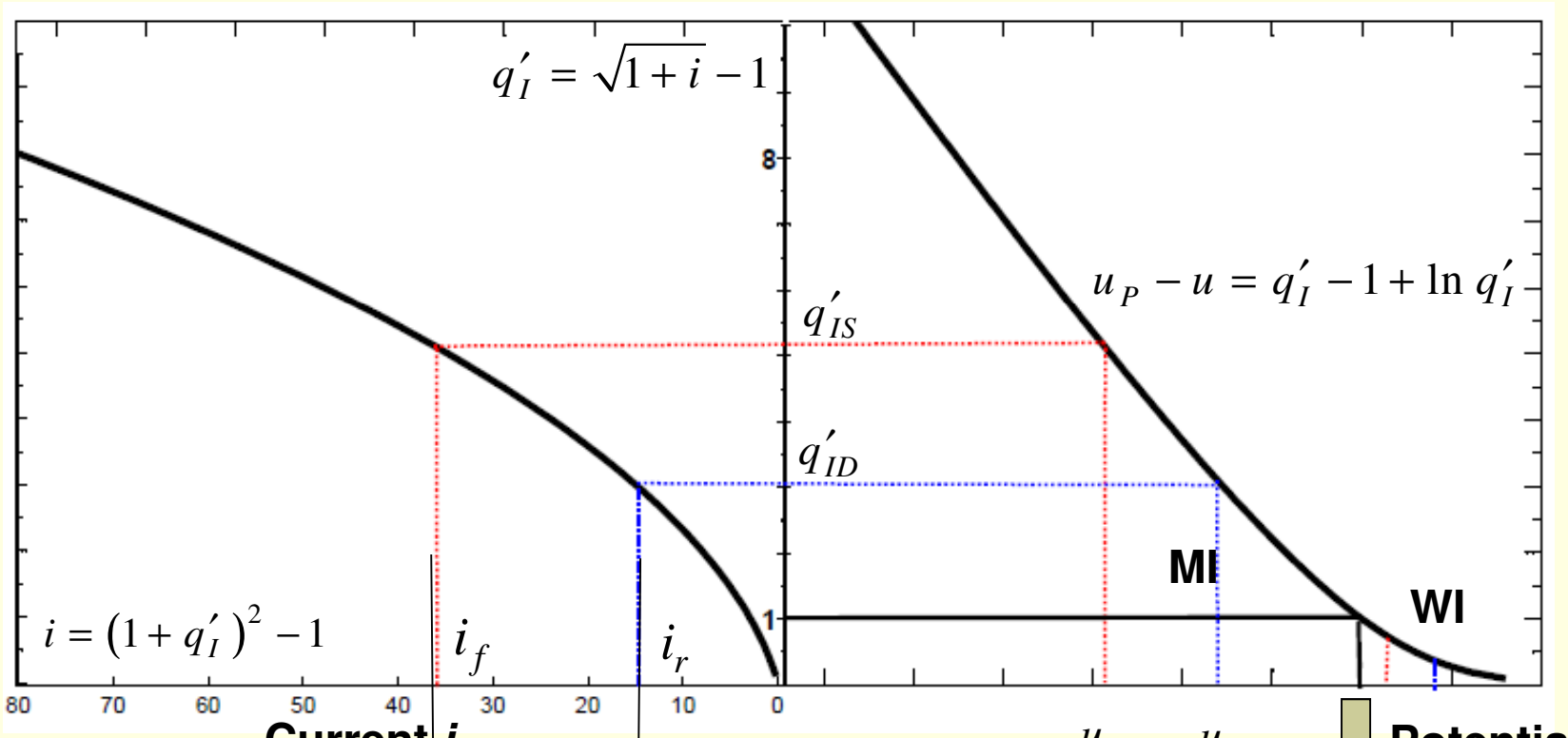
$$I_S = \mu C'_{ox} n\frac{\phi_t^2}{2}\frac{W}{L} = I_{SQ}\frac{W}{L}$$

I_S and I_{SQ} are the normalization (specific) current and the “sheet” normalization current

Normalized charge-based MOSFET model

$$u_P - u_{S(D)} = \frac{V_P - V_{S(D)}}{\phi_t} = \sqrt{1+i_{f(r)}} - 2 + \ln\left(\sqrt{1+i_{f(r)}} - 1\right)$$

Inversion charge per unit area *q'I*



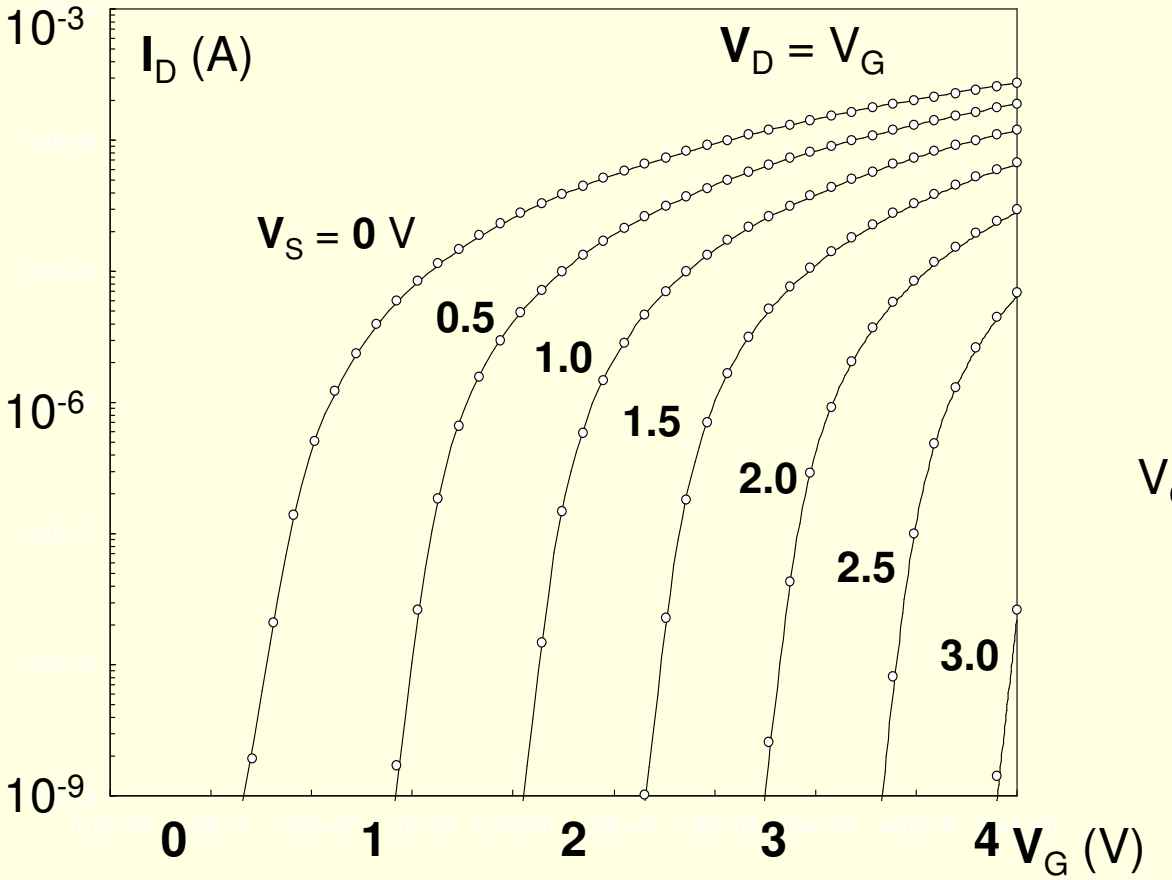
$$i_d = i_f - i_r$$

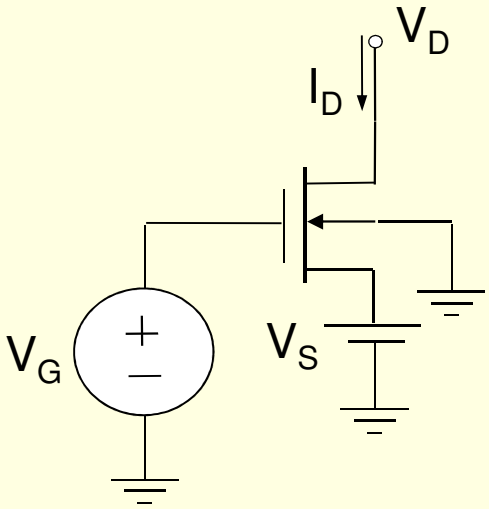
$$I_D = I_S i_d$$

$$u_P \cong \frac{u_G - u_{T0}}{n}$$

The I-V relationship

$$V_P - V_S = \phi_t \left[\sqrt{1+i_f} - 2 + \ln\left(\sqrt{1+i_f} - 1 \right) \right]$$





Common-source characteristics

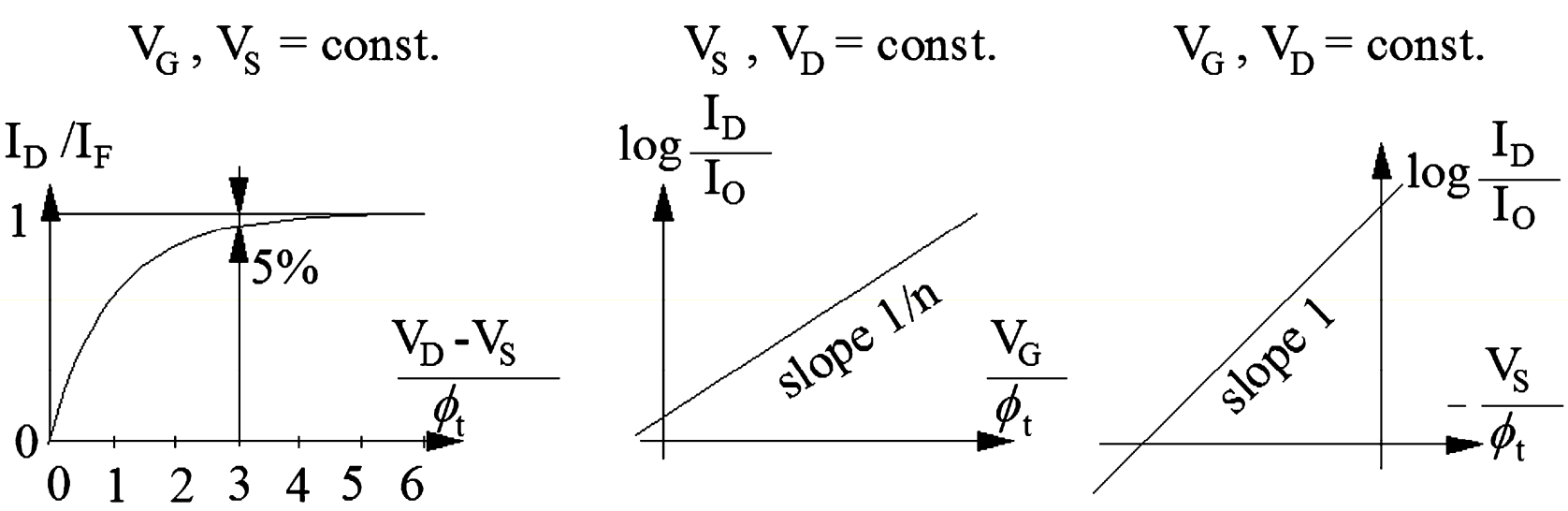
Weak inversion model

Weak inversion
$i_{f(r)}<1$

$$\frac{V_G - V_{T0}}{n} - V_{S(D)} = \phi_t \left[\underbrace{\sqrt{1+i_{f(r)}} - 2}_{-1} + \ln\left(\underbrace{\sqrt{1+i_{f(r)}} - 1}_{i_{f(r)}/2} \right) \right]$$

$$I_D = I_0 e^{\left(\frac{V_G - V_{T0}}{n} - V_S\right)/\phi_t} \left[1 - e^{-V_{DS}/\phi_t}\right]$$

$$I_0 = \mu_n \frac{W}{L} n C'_{ox} \phi_t^2 e^1 = 2 I_S e^1$$



Transconductances - 1

Transconductances $\Delta I_D = g_{mg}\Delta V_G - g_{ms}\Delta V_S + g_{md}\Delta V_D + g_{mb}\Delta V_B$

$g_{mg} - g_{ms} + g_{md} + g_{mb} = 0$

$g_{mg} = \frac{\partial I_D}{\partial V_G}, g_{ms} = -\frac{\partial I_D}{\partial V_S}, g_{md} = \frac{\partial I_D}{\partial V_D}, g_{mb} = \frac{\partial I_D}{\partial V_B}$

Calculation of g_{ms}

$$g_{ms} = -\frac{\partial (I_F - I_R)}{\partial V_S} = -\frac{\partial I_F}{\partial V_S} = -\mu \frac{W}{L} Q'_{IS}$$

$$g_{md} = -\mu \frac{W}{L} Q'_{ID}$$

UCCM

$$g_{mg} = I_S \frac{\partial (i_f - i_r)}{\partial V_G}$$

UCCM

$$\frac{\partial i_f}{\partial V_G} = -\frac{\partial i_f}{n \partial V_S}$$

$$\frac{\partial i_r}{\partial V_G} = -\frac{\partial i_r}{n \partial V_D}$$

$$g_{mg} = g_m = \frac{g_{ms} - g_{md}}{n}$$

$g_m = \frac{g_{ms}}{n}$ ⟶ in saturation

Transconductances - 2

$$g_{ms(d)} = \frac{2I_S}{\phi_t}\left(\sqrt{1+i_{f(r)}} - 1\right) = \frac{W}{L}\mu n C'_{ox}\phi_t\left(\sqrt{1+i_{f(r)}} - 1\right)$$

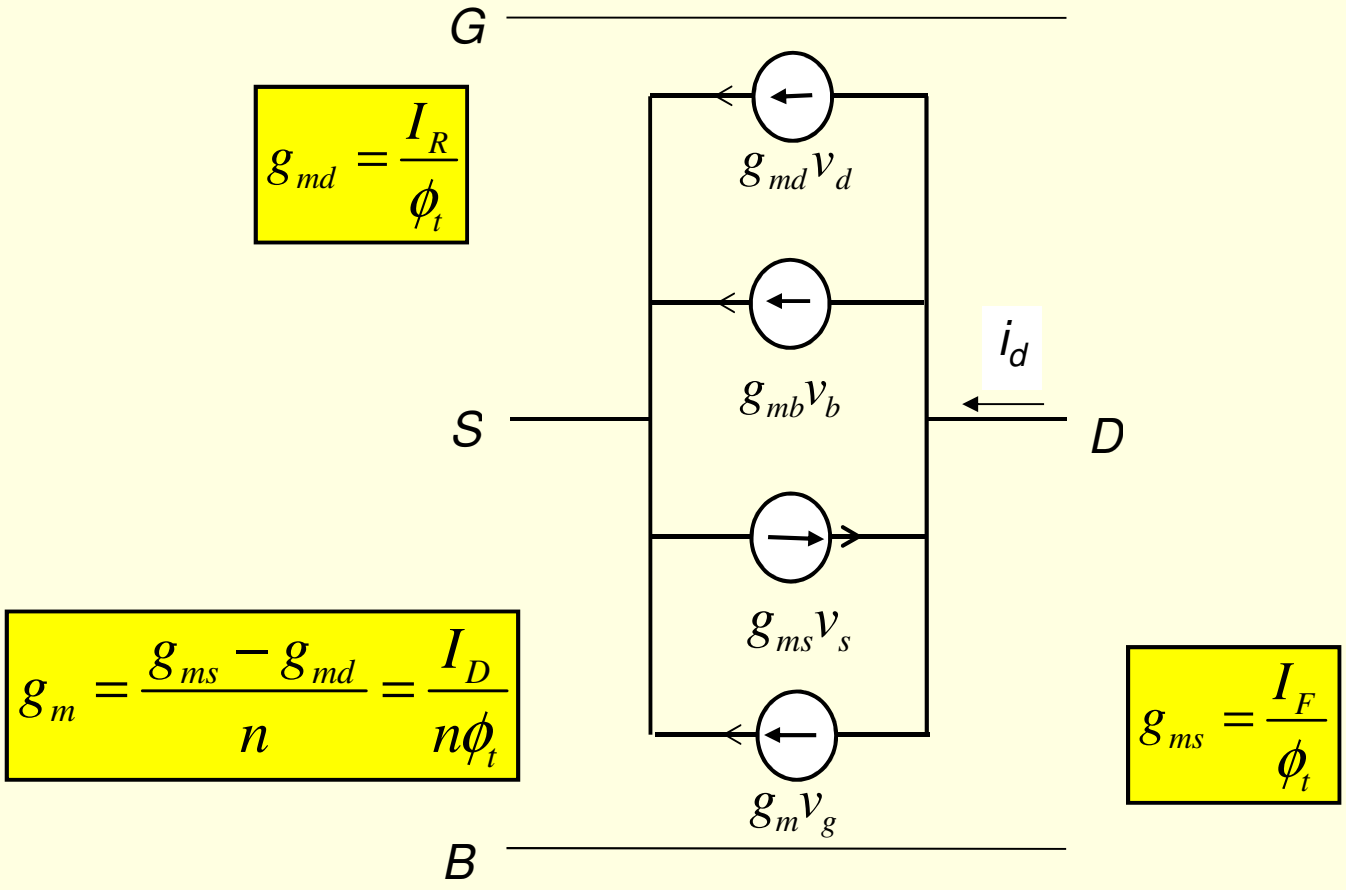
$$g_m = \frac{g_{ms} - g_{md}}{n} \qquad \frac{g_m}{I_D} = \frac{2}{n\phi_t\left(\sqrt{1+i_f} + \sqrt{1+i_r}\right)}$$

For $V_{DS}/\phi_t << 1$ we have $i_f \cong i_r$

In saturation

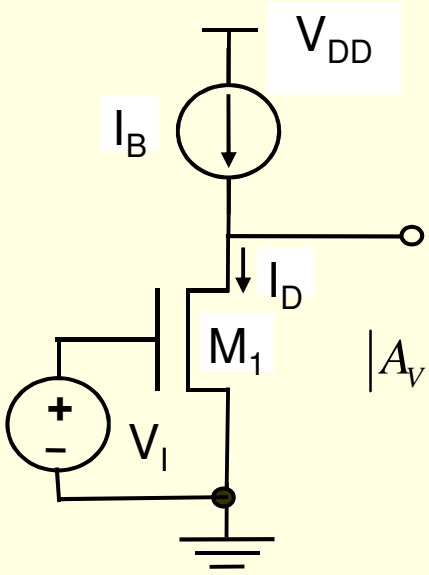
$$\frac{g_m}{I_D} \cong \frac{1}{n\phi_t\sqrt{1+i_f}} \qquad \frac{g_m}{I_D} = \frac{2}{n\phi_t\left(\sqrt{1+i_f} + 1\right)}$$

MOSFET: low-frequency small-signal model in weak inversion



$$g_{ms} = g_m + g_{mb} + g_{md}$$

Low-voltage operation of the common-source amplifier



Intrinsic gain stage

(I_B ideal current source)

weak inversion operation

$$|A_V| = \frac{g_m}{g_{md}} = \frac{g_{ms} - g_{md}}{n g_{md}} = \frac{1}{n}\left(\frac{g_{ms}}{g_{md}} - 1\right)$$

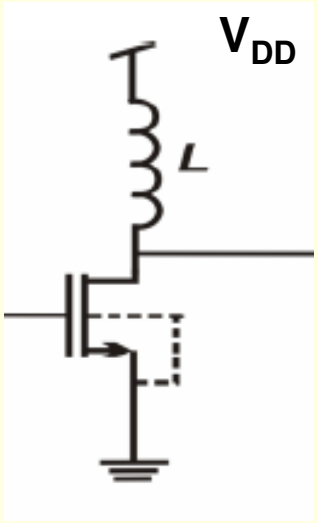
$$\frac{g_{ms}}{g_{md}} = e^{\frac{V_{DS}}{\phi_t}}$$

$$|A_V| = \frac{1}{n}\left(e^{\frac{V_{DS}}{\phi_t}} - 1\right)$$

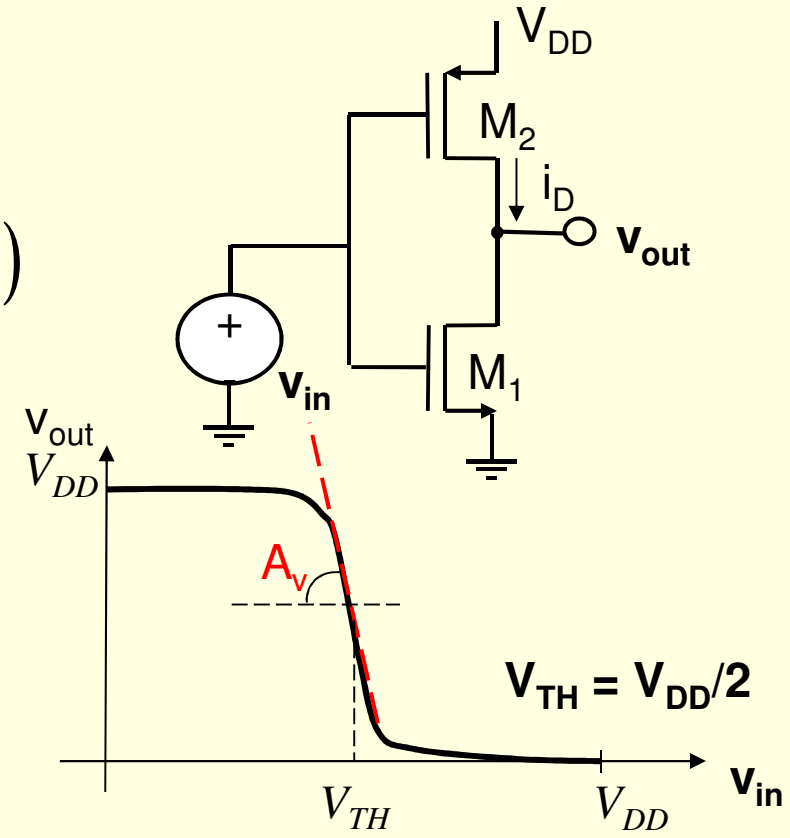
or

$$V_{DS} = \phi_t \ln\left(1 + n|A_V|\right)$$

Low–voltage operation of the (C)MOS inverter



$$V_{DS} = \phi_t \ln\left(1 + n\left|A_V\right|\right)$$



Minimum supply voltage for amplification $\left|A_V\right| = 1$

'ideal' MOSFET *n* = 1

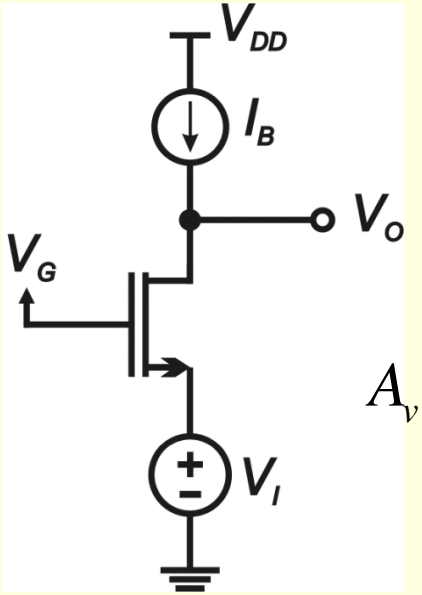
$$V_{DS} = V_{DD}$$

$$V_{DD\min} = (\ln 2)\phi_t$$

$$V_{DS} = V_{DD} / 2$$

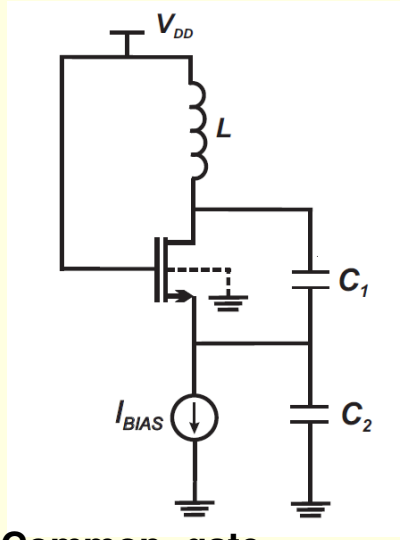
$$V_{DD\min} = 2(\ln 2)\phi_t$$

Low-voltage operation of the common-gate amplifier



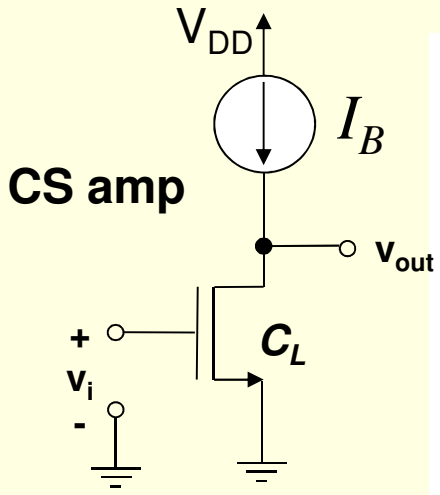
$$A_{v,cg} = \frac{v_o}{v_i} = \frac{g_{ms}}{g_{md}} = e^{\frac{qV_{DS}}{kT}}$$

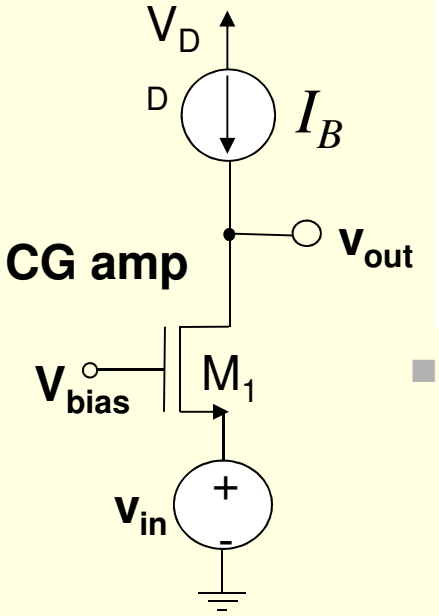
The common-gate amplifier provides a voltage gain of greater than unity for $V_{DS}>0$. → Very useful property for lowering the supply voltage limit for the operation of oscillators (later).

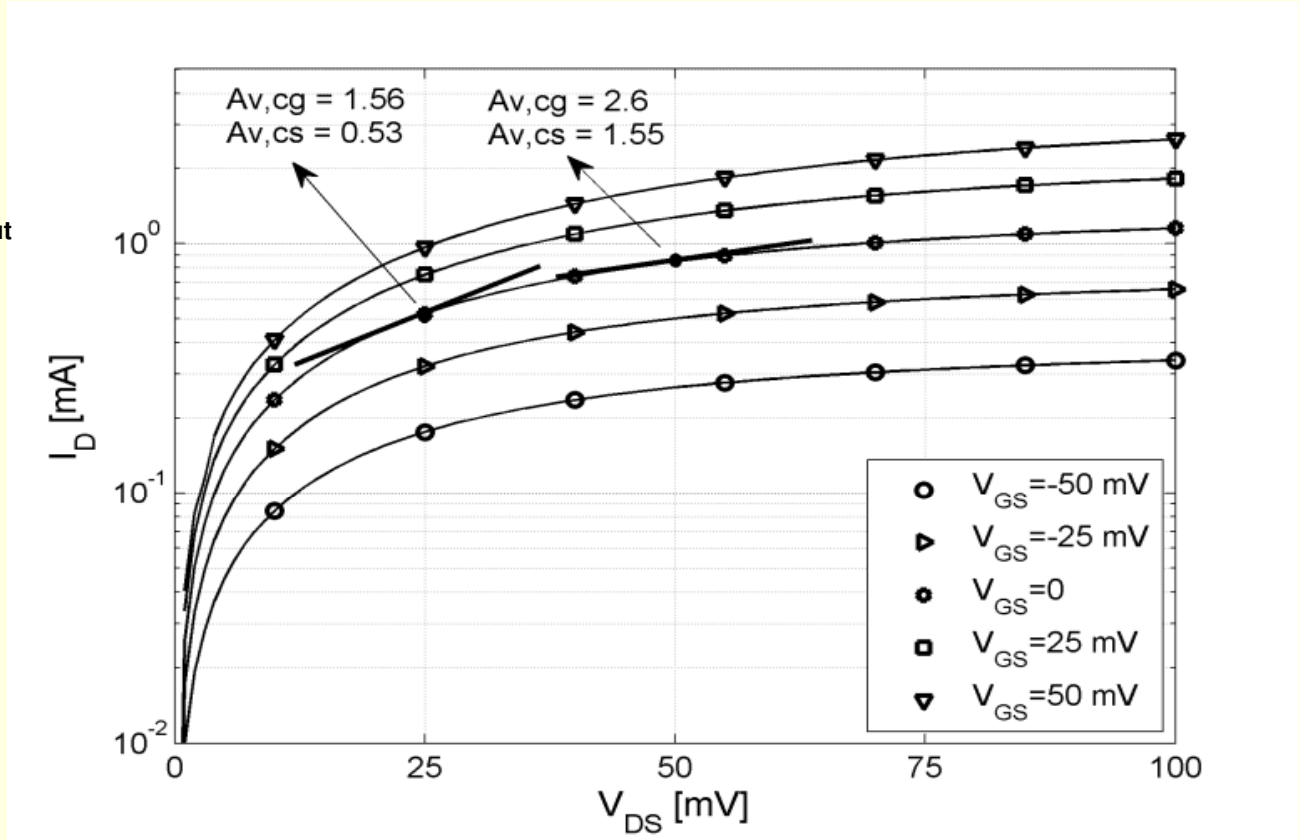


Common- gate Colpitts oscillator

Zero-VT MOSFETs







- I_D x V_{DS} (V_S=V_B) characteristics for a zero-VT transistor with W/L=2500µm/420nm. For V_{GS}= 0 V and V_{DS}= 25 mV the values of the common-gate and common-source gains are 1.56 and 0.53, respectively.

ULTRA-LOW-VOLTAGE (ULV) IC DESIGN: DESIGNING FOR VDD BELOW kT/q

Chapter 2

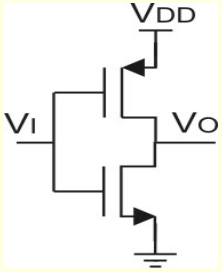
Ultra-Low-Voltage (ULV)

CMOS logic circuits

THE CMOS INVERTER

Static Analysis in weak inversion 1

$$I_{DN(P)} = I_{ON(P)} \cdot e^{\frac{V_{GB(BG)} - \left|V_{TN(P)}\right| - n_N \cdot V_{SB(BS)}}{n_{N(P)} \cdot \phi_t}} \cdot \left(1 - e^{-\frac{V_{DS(SD)}}{\phi_t}}\right)$$



- The strength or current capability of the transistor is given by

$$I_{N(P)} = I_{ON(P)} \cdot e^{\frac{-\left|V_{TN(P)}\right|}{n_{N(P)} \cdot \phi_t}}$$

- For the sake of simplicity let $n_N = n_P = n$. The static transfer function of the inverter is obtained from

$$I_{DN} = I_{DP}$$

$$I_{ON} \cdot e^{\frac{V_I - V_{TN}}{n \cdot \phi_t}} \cdot \left(1 - e^{-\frac{V_O}{\phi_t}}\right) = I_{OP} \cdot e^{\frac{V_{DD} - V_I - \left|V_{TP}\right|}{n \cdot \phi_t}} \cdot \left(1 - e^{-\frac{V_{DD} - V_O}{\phi_t}}\right)$$

THE CMOS INVERTER

Static Analysis in weak inversion 2

$$V_I = \frac{V_{DD}}{2} + \frac{V_{TN} - |V_{TP}|}{2} + \frac{n \cdot \phi_t}{2} \cdot \ln\left(\frac{I_{OP}}{I_{ON}}\right) + \frac{n \cdot \phi_t}{2} \cdot \ln\left(\frac{1 - e^{-\frac{V_{DD} - V_O}{\phi_t}}}{1 - e^{-\frac{V_O}{\phi_t}}}\right)$$

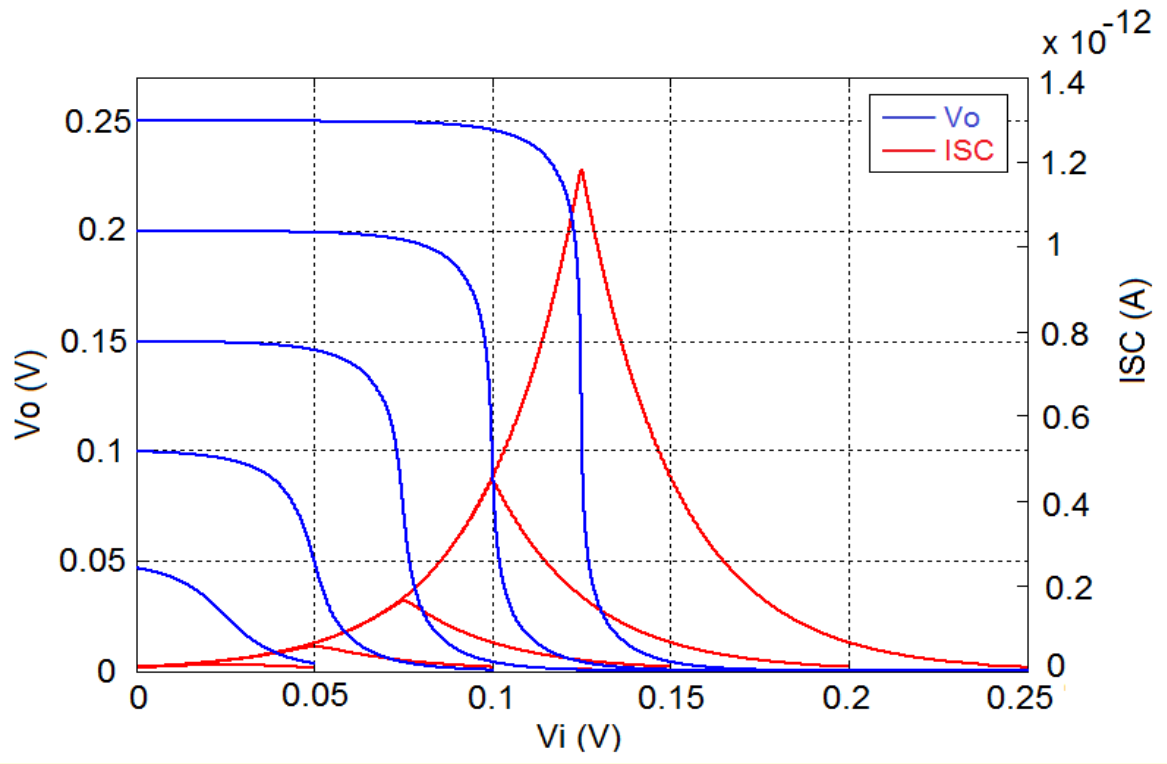
In the ideal case of NMOS and PMOS transistors with the same strength, i.e. $I_{ON}=I_{OP}$ and $V_{TN}=|V_{TP}|$, the VTC reduces to

$$V_I = \frac{V_{DD}}{2} + \frac{n \cdot \phi_t}{2} \cdot \ln\left(\frac{1 - e^{-\frac{V_{DD} - V_O}{\phi_t}}}{1 - e^{-\frac{V_O}{\phi_t}}}\right)$$

$$I_{SC} = \sqrt{I_{ON} \cdot I_{OP}} \cdot e^{\frac{V_{DD} - V_{TN} - |V_{TP}|}{2 \cdot n \cdot \phi_t}} \cdot \sqrt{\left(1 - e^{-\frac{V_O}{\phi_t}}\right) \cdot \left(1 - e^{-\frac{V_{DD} - V_O}{\phi_t}}\right)}$$

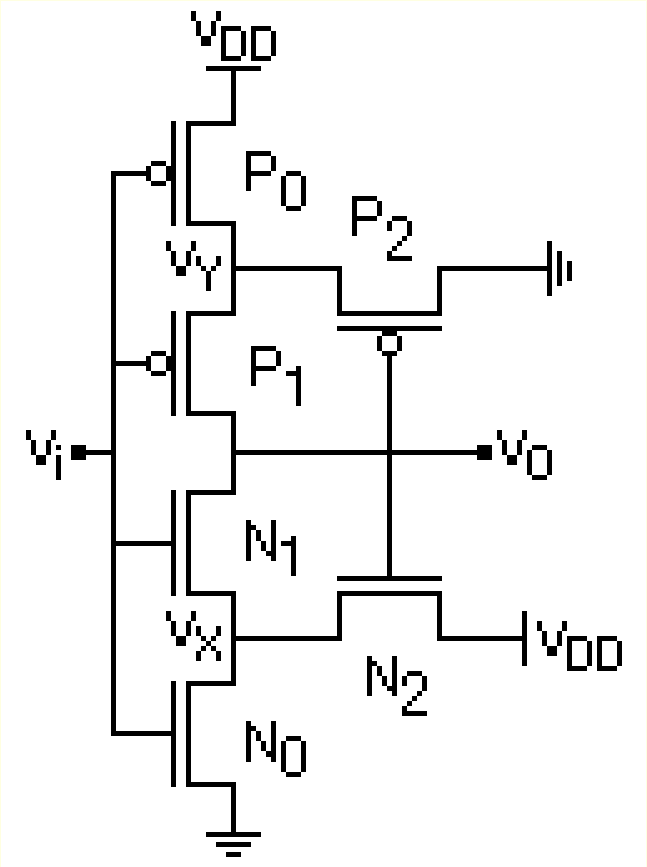
THE CMOS INVERTER

Static Analysis in weak inversion 3



- Inverter voltage and current transfer characteristics.

SCHMITT TRIGGER ANALYSIS



Schmitt Trigger Inverter

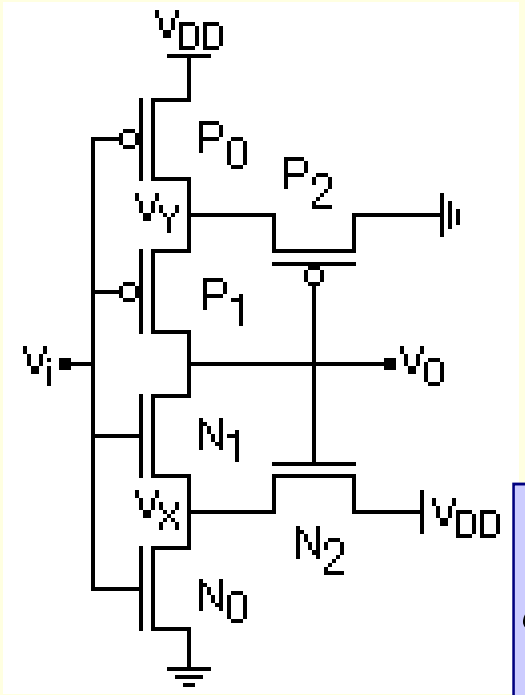
- *2 internal nodes (V_X and V_Y)*
- *Feedback transistors controlled by the output*
- *Hysteresis for VDD > 80mV*
- *No hysteresis is desired for VDD minimization*
- *For symmetric operation, corresponding NMOS and PMOS MOSFETs have the same current capability*

ST ANALYSIS – DC TRANSFER 1

MOSFET current in weak inversion:

$$I_{DN(P)} = I_{ON(P)} \cdot e^{\frac{V_{GB(BG)} - n_{N(P)} \cdot V_{SB(BS)}}{n_{N(P)} \cdot \phi_t}} \cdot \left(1 - e^{-\frac{V_{DS(SD)}}{\phi_t}}\right)$$

$$n_{N(P)} = 1$$



$$e^{\frac{V_Y}{\phi_t}} = \frac{I_0 \cdot e^{\frac{V_{DD}}{\phi_t}} + I_1 \cdot e^{\frac{V_O}{\phi_t}} + I_2 \cdot e^{\frac{V_I - V_O}{\phi_t}}}{I_0 + I_1 + I_2 \cdot e^{\frac{V_I - V_O}{\phi_t}}}$$

$$e^{\frac{V_I - V_X}{\phi_t}} - e^{\frac{V_I - V_O}{\phi_t}} = e^{\frac{V_Y - V_I}{\phi_t}} - e^{\frac{V_O - V_I}{\phi_t}}$$

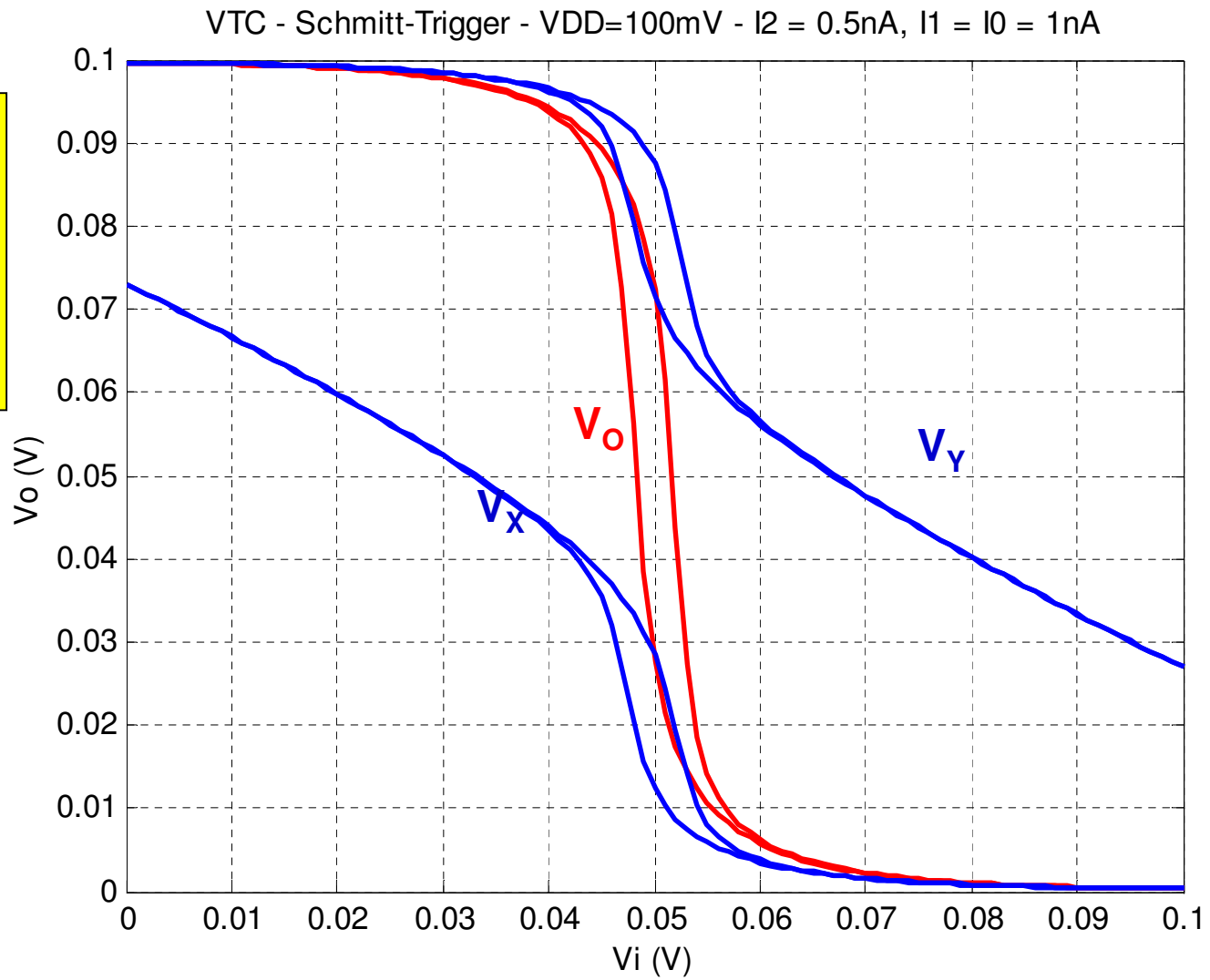
$$e^{\frac{V_X}{\phi_t}} = \frac{I_0 + I_1 + I_2 \cdot e^{\frac{V_O - V_I}{\phi_t}}}{I_0 + I_1 \cdot e^{-\frac{V_O}{\phi_t}} + I_2 \cdot e^{\frac{V_O - V_I}{\phi_t}} \cdot e^{-\frac{V_{DD}}{\phi_t}}}$$

Solved for Vo

Shows Hysteresis

ST ANALYSIS – DC TRANSFER 2

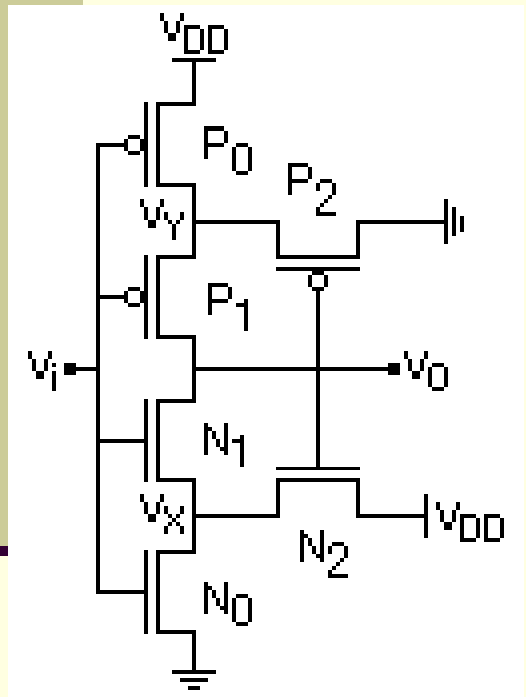
$$V_{DD} = 100mV$$
$$\frac{I_2}{I_0} = 0.5$$
$$\frac{I_1}{I_0} = 1$$



ST OPTIMIZATION 1

Series transistor: I1/I0

Rearranging the AC gain equation for I1/I0



$$\left.\frac{v_o}{v_i}\right|_{V_O=V_I=\frac{V_{DD}}{2}} = -\frac{\frac{I_1}{I_0}A_1 + B_1}{\frac{I_1}{I_0}C_1 + D_1}$$

Bilinear function with negative pole

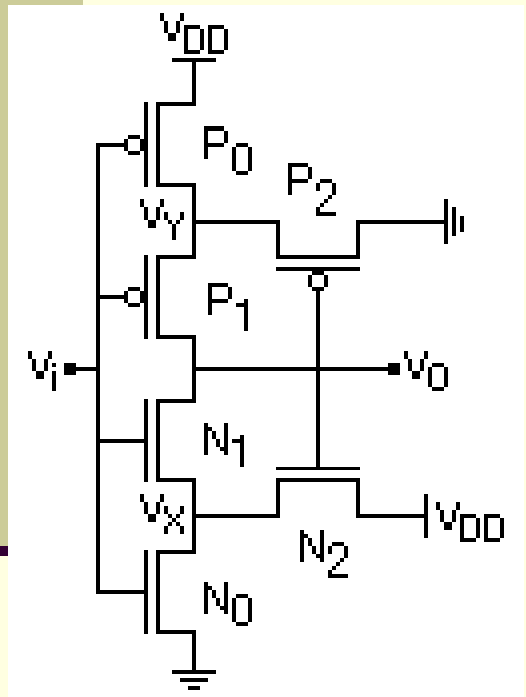
$$\left.\frac{I_1}{I_0}\right|_{OPTIMUM} = 0$$

Practical values of I1/I0 range from 0.01 to 0.1, with only slight penalty in terms of the gain.

ST OPTIMIZATION 2

Feedback transistors

Rearranging the AC gain equation for I_2/I_0



$$\left.\frac{v_o}{v_i}\right|_{V_O=V_I=\frac{V_{DD}}{2}} = -\frac{\left(\frac{I_2}{I_0}\right)^2 A_2 + \left(\frac{I_2}{I_0}\right) B_2 + C_2}{\left(\frac{I_2}{I_0}\right)^2 D_2 + \left(\frac{I_2}{I_0}\right) E_2 + F_2}$$

$$\left.\frac{I_2}{I_0}\right|_{OPTIMUM} = \frac{\sqrt{1+e^{\frac{V_{DD}}{2\phi_t}} - e^{-\frac{V_{DD}}{2\phi_t}}} - 1}{1+e^{-\frac{V_{DD}}{2\phi_t}}}$$

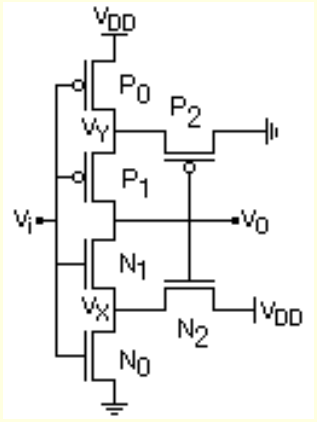
ST x CMOS INVERTER 1

73 is the best number !

Substituting the optimum values of I_1/I_0 and I_2/I_0, the ST minimum operating voltage can be calculated:

$$V_{DD\min} = 2\phi_t \ln\left(\frac{1}{\sqrt{73}-8}\right) = 31.5\text{mV at } 300\text{K}$$

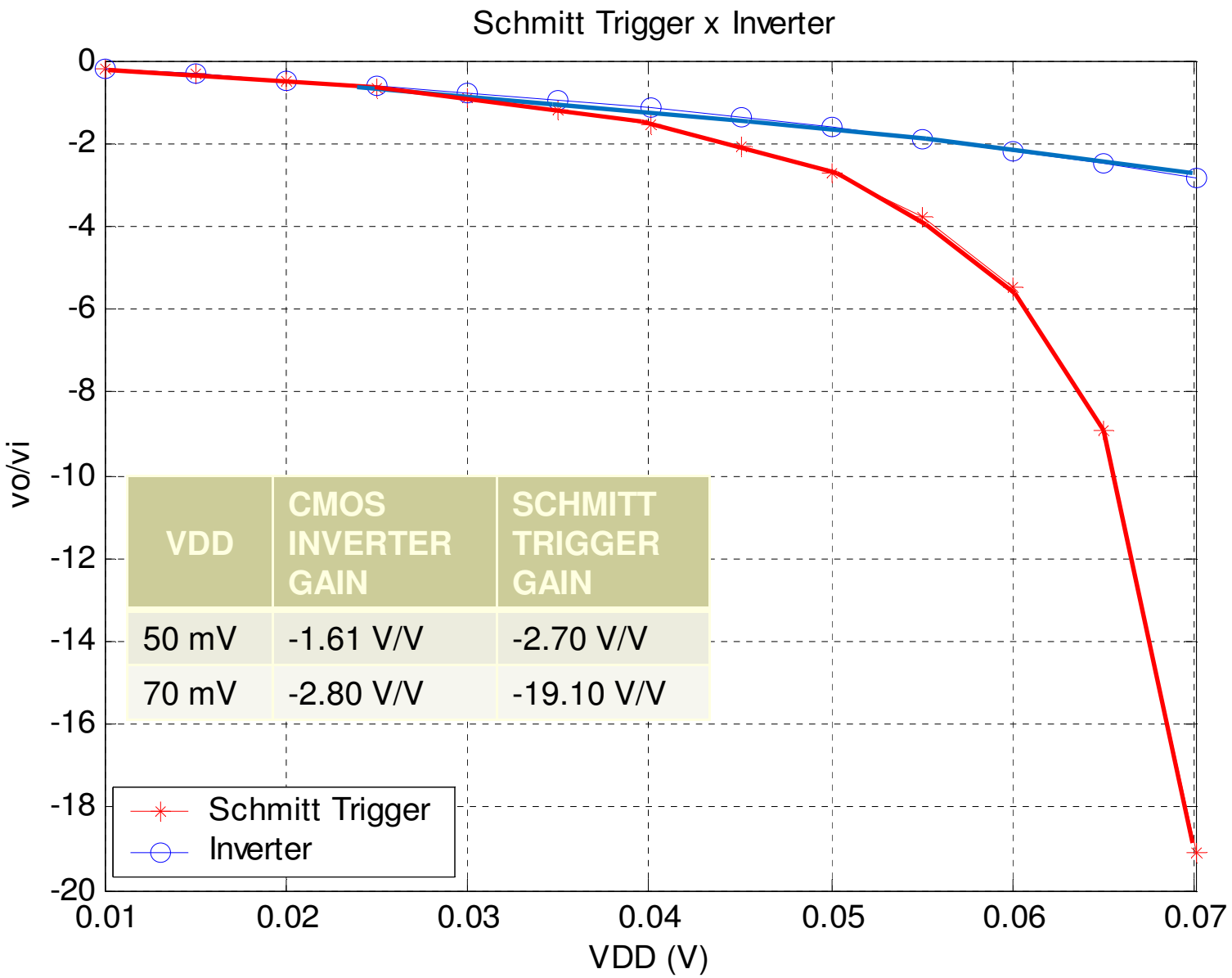
$$\left.\frac{I_1}{I_0}\right|_{OPTIMUM} = 0 \qquad \left.\frac{I_2}{I_0}\right|_{OPTIMUM} = 0.333$$



Schmitt Trigger inverter

ST structures are capable of operating at lower supply voltages than the standard static logic!!!!

ST x CMOS INVERTER 2



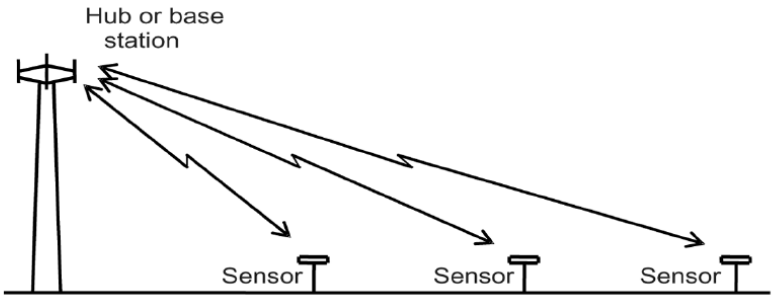
VDD	CMOS INVERTER GAIN	SCHMITT TRIGGER GAIN
50 mV	-1.61 V/V	-2.70 V/V
70 mV	-2.80 V/V	-19.10 V/V

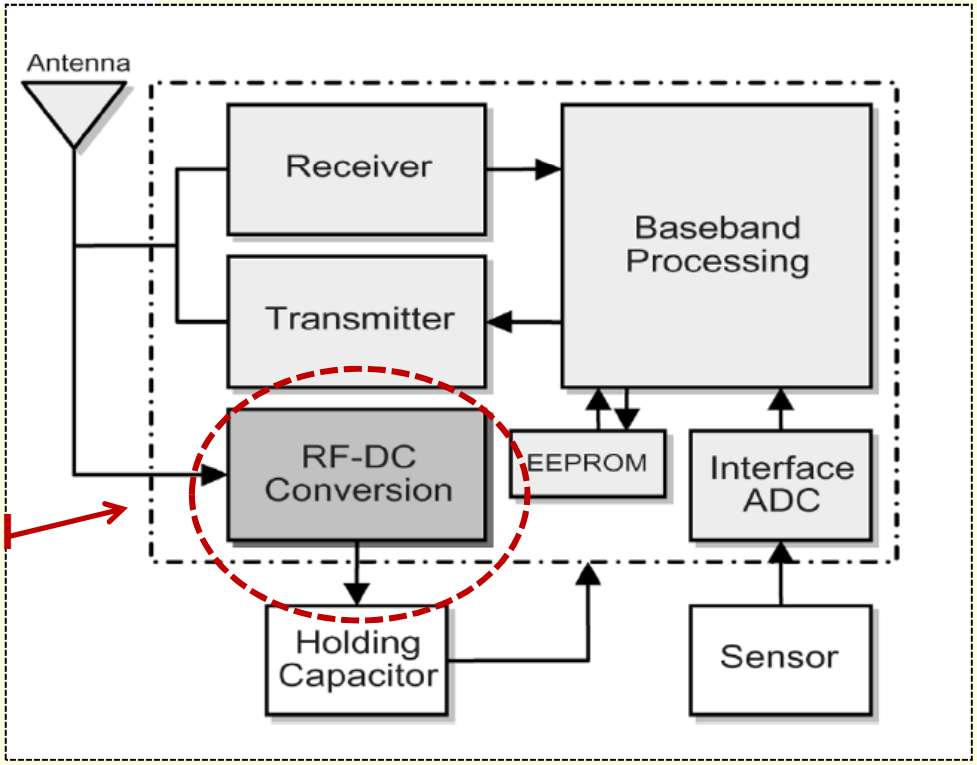
ULTRA-LOW-VOLTAGE (ULV) IC DESIGN: DESIGNING FOR VDD BELOW kT/q

Chapter 3
Ultra-Low-Voltage (ULV) rectifiers

MOTIVATION

Wirelessly powered sensors

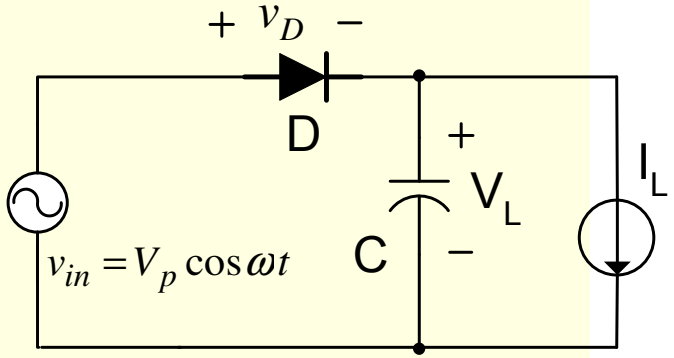


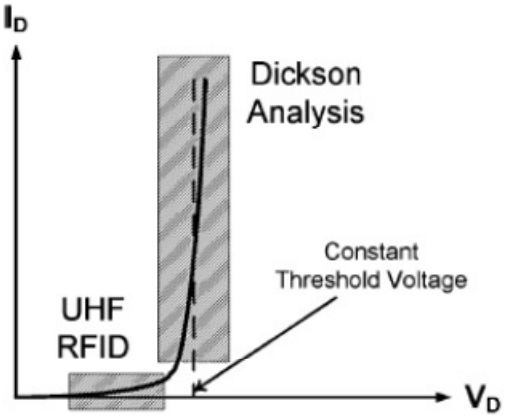


Low power/voltage level

Ultra-low-voltage diode circuits

Dickson analysis of voltage multipliers: constant threshold voltage diode model, but it is not appropriate for low voltage operation





$V_L = V_P - V_{ON}$

How to substitute the constant 'diode voltage drop' model?

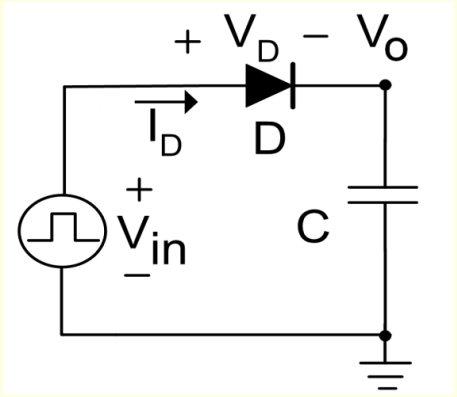
Use the i-v characteristic of the diode and the load current

$$I_D = I_S[e^{\frac{V_D}{n\phi_t}} - 1]$$

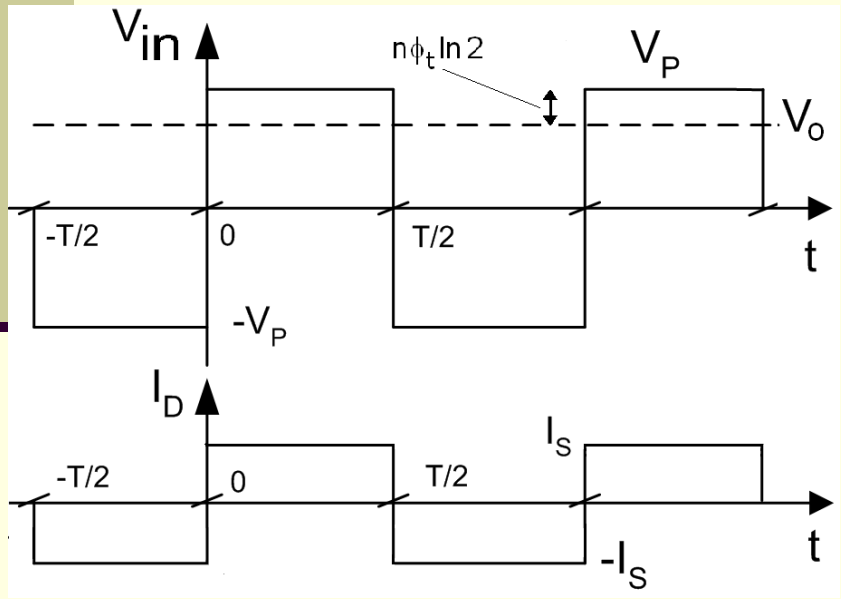
$$\phi_t = \frac{kT}{q}$$

$n \sim 1$ to 1.5

Voltage rectifier with pure capacitive load - 1



$V_P >> n\phi_t$



Steady-state analysis

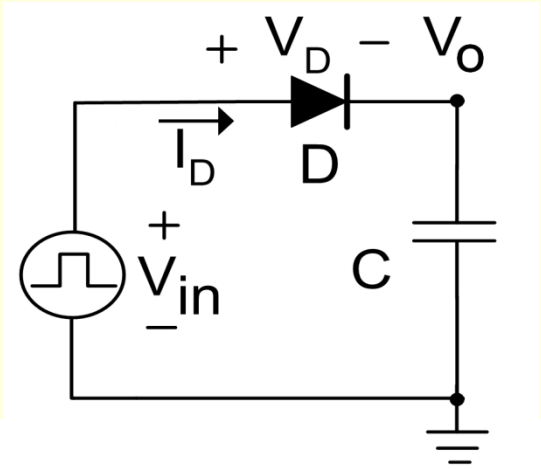
$$\frac{1}{T}\int_{-T/2}^{T/2} I_D\,dt = 0 \qquad I_D = I_S\left[e^{\frac{V_D}{n\phi_t}} - 1\right]$$

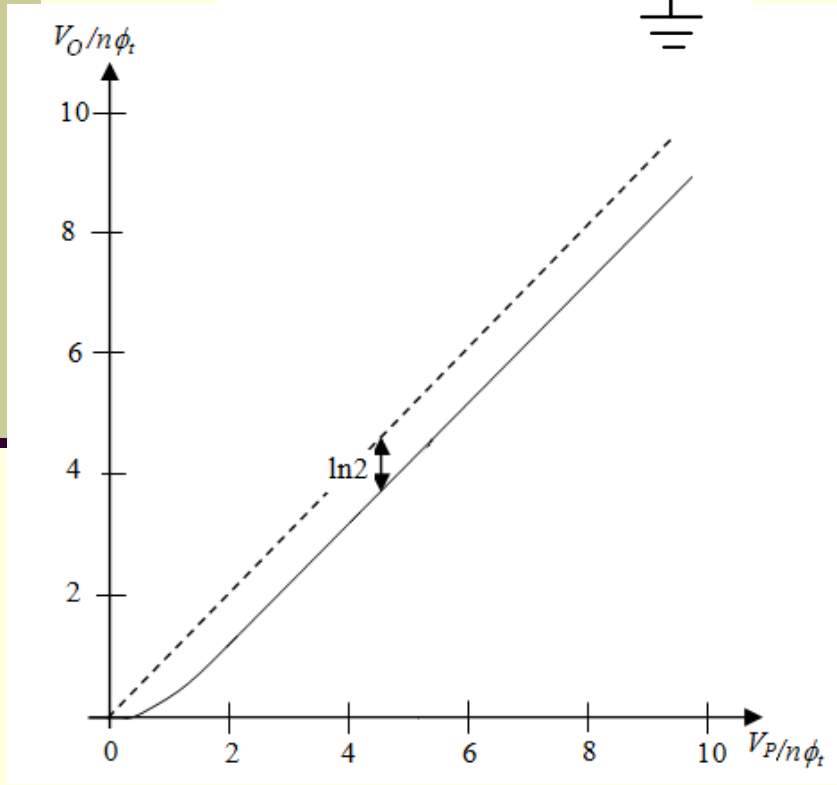
$$\frac{I_S}{T}\left[\int_{-T/2}^{0}\left(e^{\left(\frac{-V_P - V_o}{n\phi_t}\right)} - 1\right)dt + \int_{0}^{T/2}\left(e^{\left(\frac{V_P - V_o}{n\phi_t}\right)} - 1\right)dt\right] = 0$$

Assumption: very low ripple (high C)
→ V_o ≅ constant

$$\frac{V_o}{n\phi_t} = \ln\left[\frac{e^{V_P/n\phi_t} + e^{-V_P/n\phi_t}}{2}\right] = \ln\left[\cosh\left(V_P/n\phi_t\right)\right]$$

Voltage rectifier with pure capacitive load - 2





$$\frac{V_o}{n\phi_t} = \ln\left[\cosh\left(V_P/n\phi_t\right)\right]$$

Power Detector

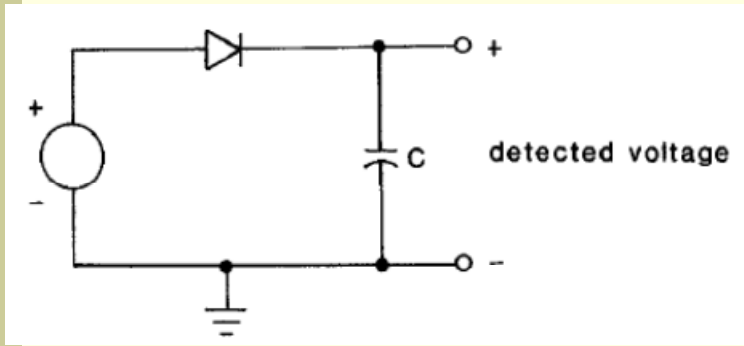
$$V_P \ll n\phi_t \quad \rightarrow \quad \frac{V_o}{n\phi_t} \cong \frac{1}{2}\left(\frac{V_P}{n\phi_t}\right)^2$$

Peak Detector **Diode "ON" voltage drop**

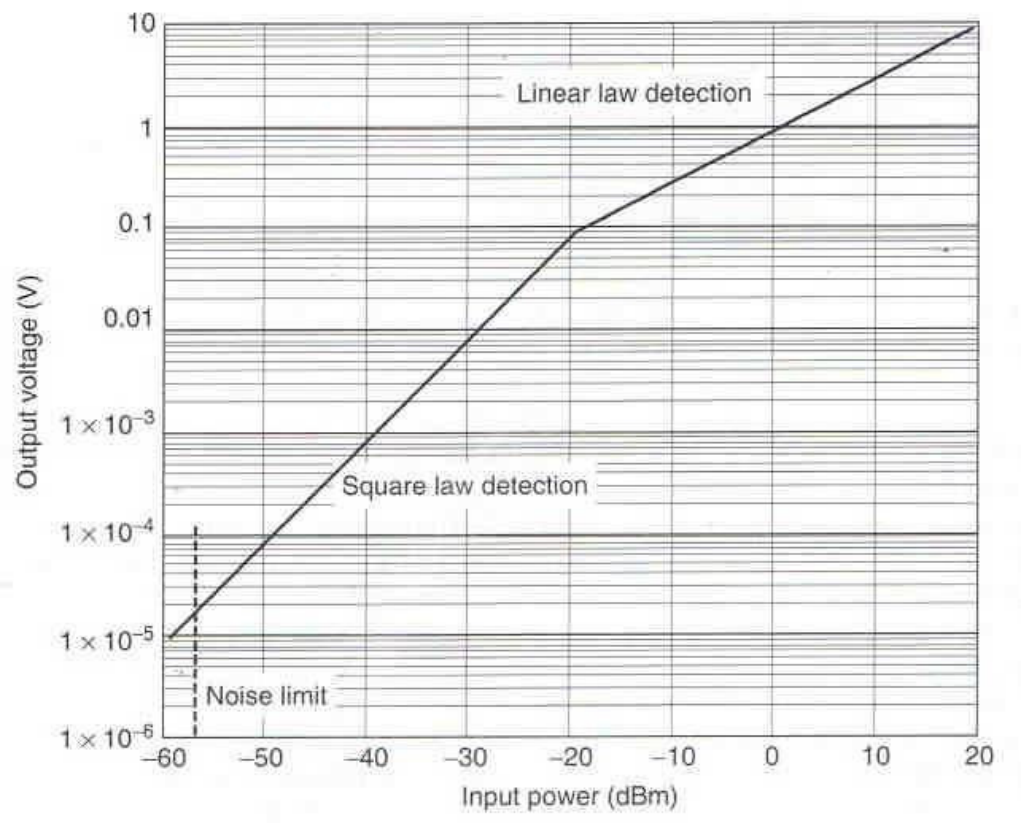
$$V_P \gg n\phi_t \quad \rightarrow \quad V_L \cong V_P - n\phi_t \ln 2$$

Input

Application: microwave power detection



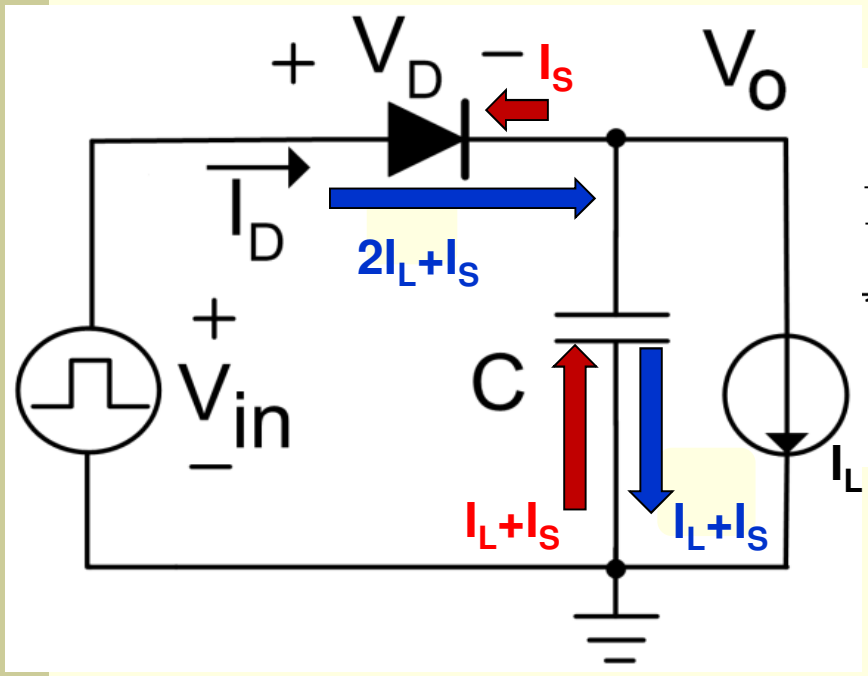
- Basic detector circuit



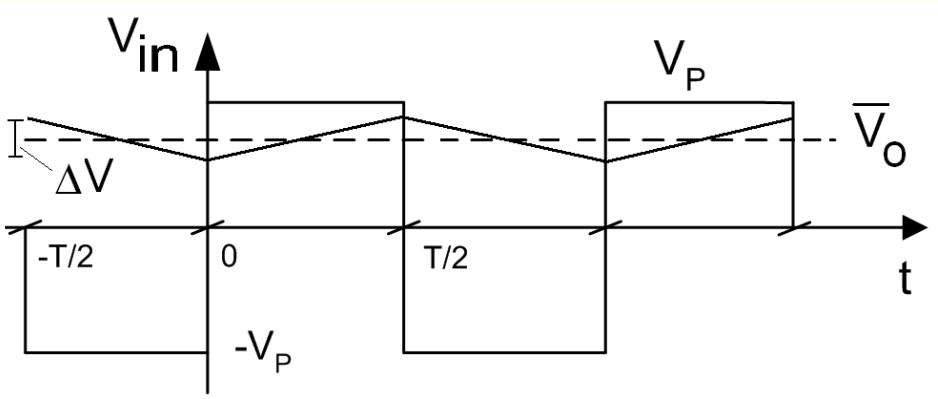
R. G. Meyer, " Low-power monolithic RF peak detector analysis, " IEEE J. Solid-State Circuits, vol. 30, no. 1, pp. 65–67, Jan. 1995.

Wetenkamp, IEEE MTT-S Int. Microwave Symp. Dig., 1983

Voltage rectifier with DC load - 1



Output voltage ripple

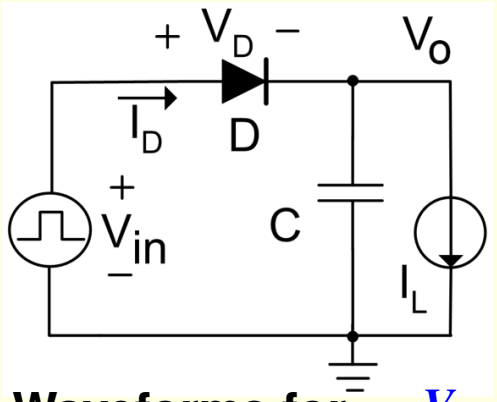


The discharge rate of the capacitor

$$I_C = \frac{dQ_C}{dt} = C\frac{dV_C}{dt} \cong I_L + I_S$$

$$\int_{-T/2}^{0} dV_C = \Delta V \cong \frac{I_L + I_S}{C}\frac{T}{2} = \frac{I_L + I_S}{2fC}$$

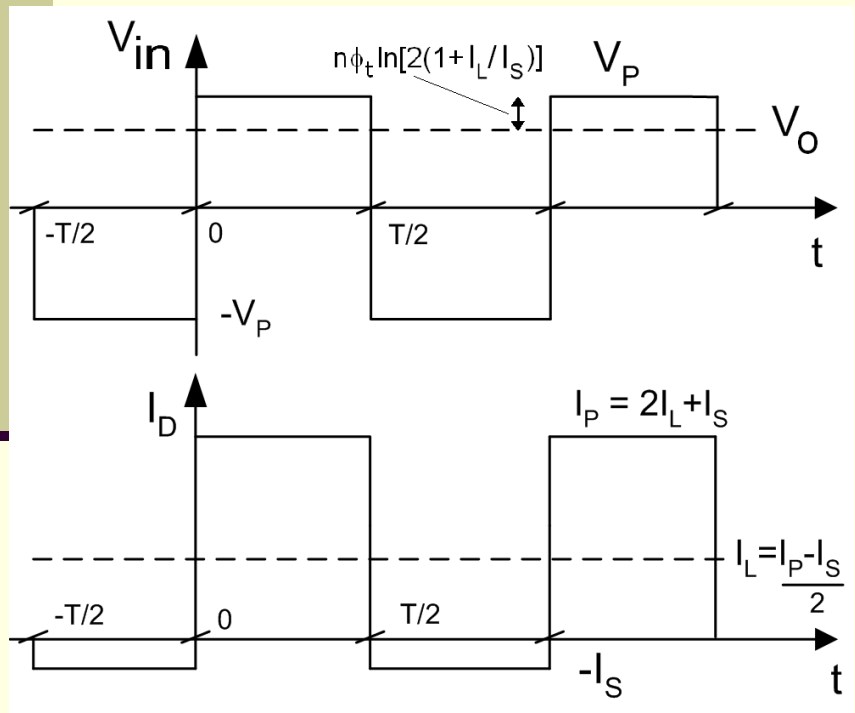
Voltage rectifier with DC load - 2



Steady-state analysis

$$\frac{I_S}{T}\left[\int_{-T/2}^{0}\left(e^{\left(\frac{-V_P-V_o}{n\phi_t}\right)}-1\right)dt+\int_{0}^{T/2}\left(e^{\left(\frac{V_P-V_o}{n\phi_t}\right)}-1\right)dt\right]=I_L$$

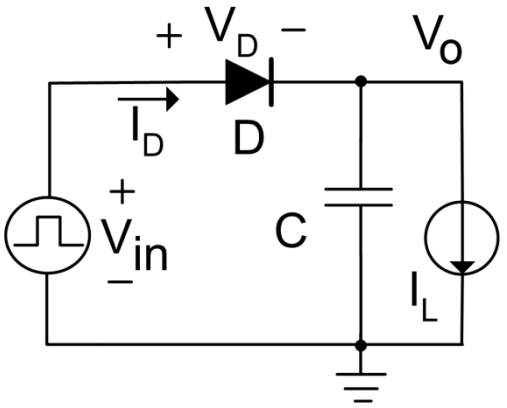
Waveforms for $V_P >> n\phi_t$



Assumption: very low ripple → V_o ≅ constant

$$\frac{V_o}{n\phi_t}=\ln\left[\frac{\cosh\left(V_P/n\phi_t\right)}{1+I_L/I_S}\right]$$

Voltage rectifier with DC load - 3

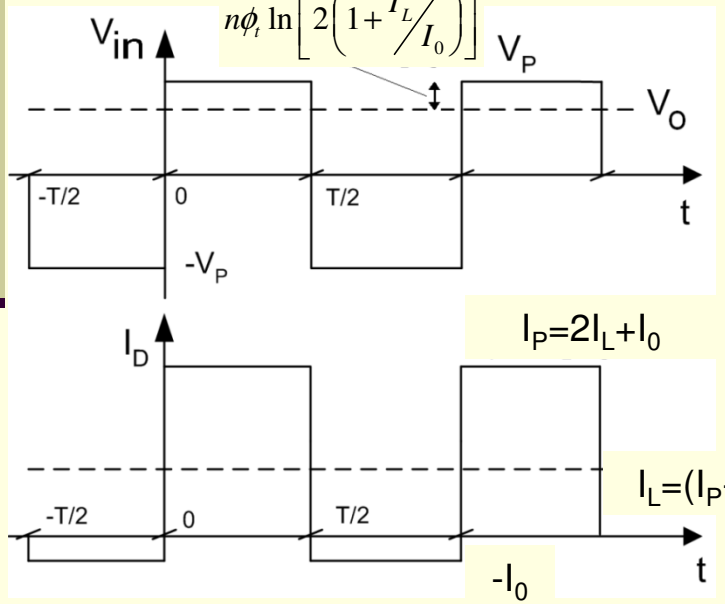


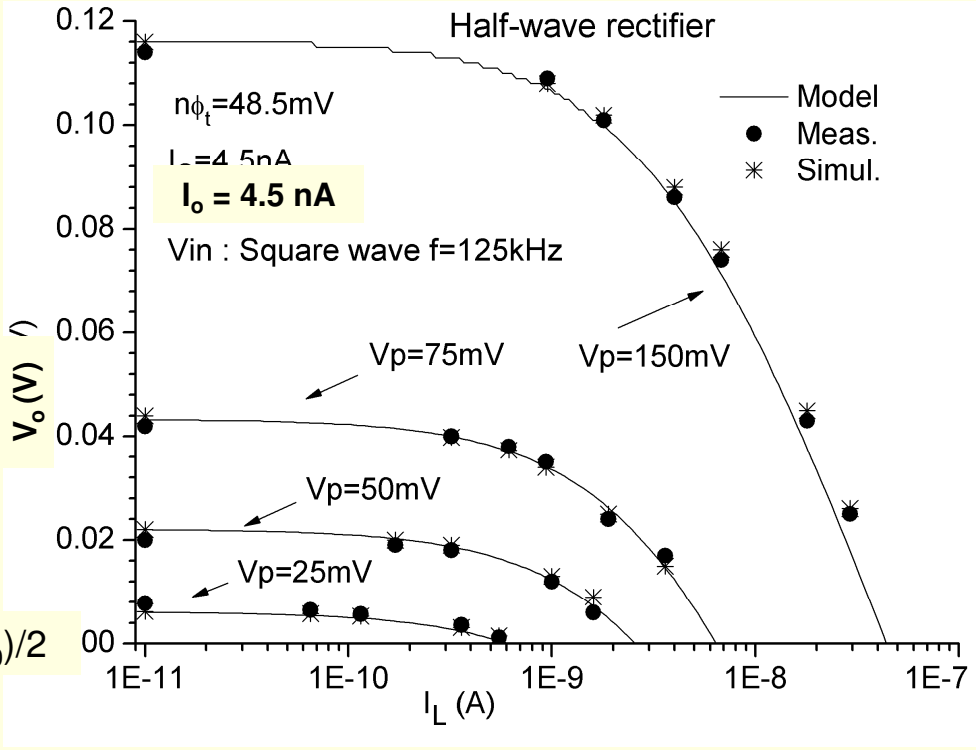
Input

Diode "ON" voltage drop

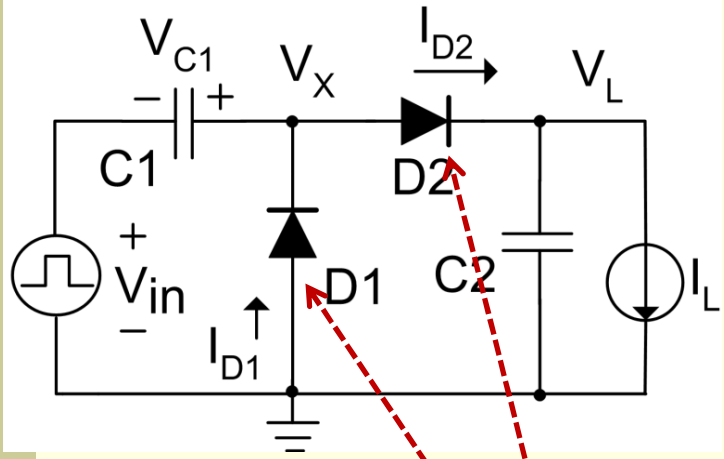
$$V_P > n\phi_t \quad \rightarrow \quad V_o \cong V_P - n\phi_t \ln\left(\frac{I_P + I_0}{I_0}\right)$$

Waveforms for $V_P >> n\phi_t$





The voltage doubler



$$PCE = \frac{P_{load}}{P_{in}} = \frac{V_L I_L}{P_{load} + P_{loss}}$$

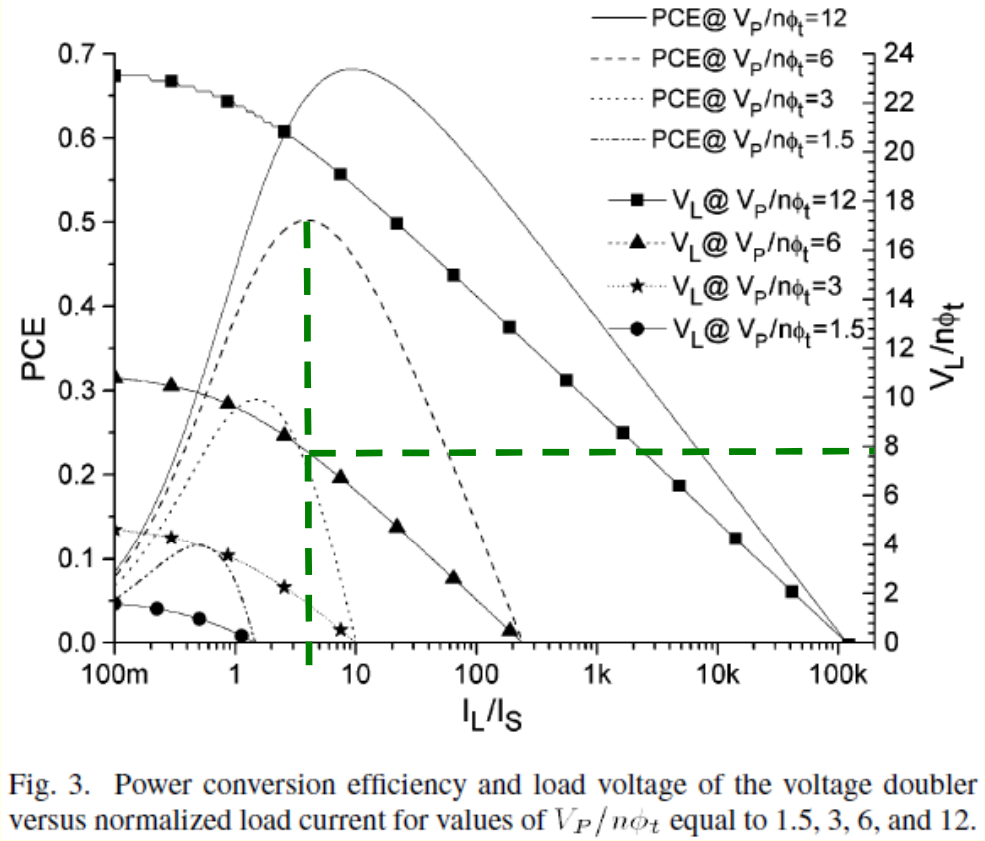
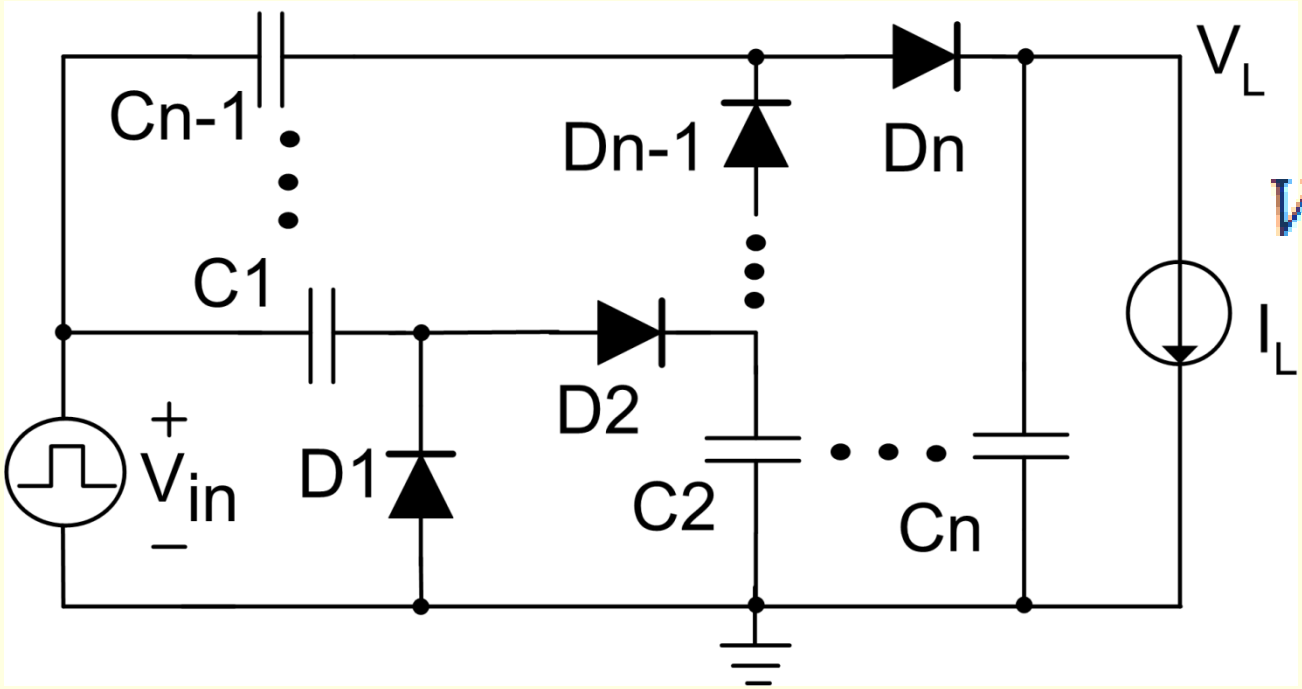


Fig. 3. Power conversion efficiency and load voltage of the voltage doubler versus normalized load current for values of $V_P/n\phi_t$ equal to 1.5, 3, 6, and 12.

PCE: Power Conversion Efficiency

$$PCE = \frac{P_{out}}{P_{out} + P_{loss}} \cong \frac{1 - \frac{n\phi_t}{V_P} \ln\left[2\left(1 + I_L / I_S\right)\right]}{\left(1 + I_S / I_L\right)}$$

The voltage multiplier



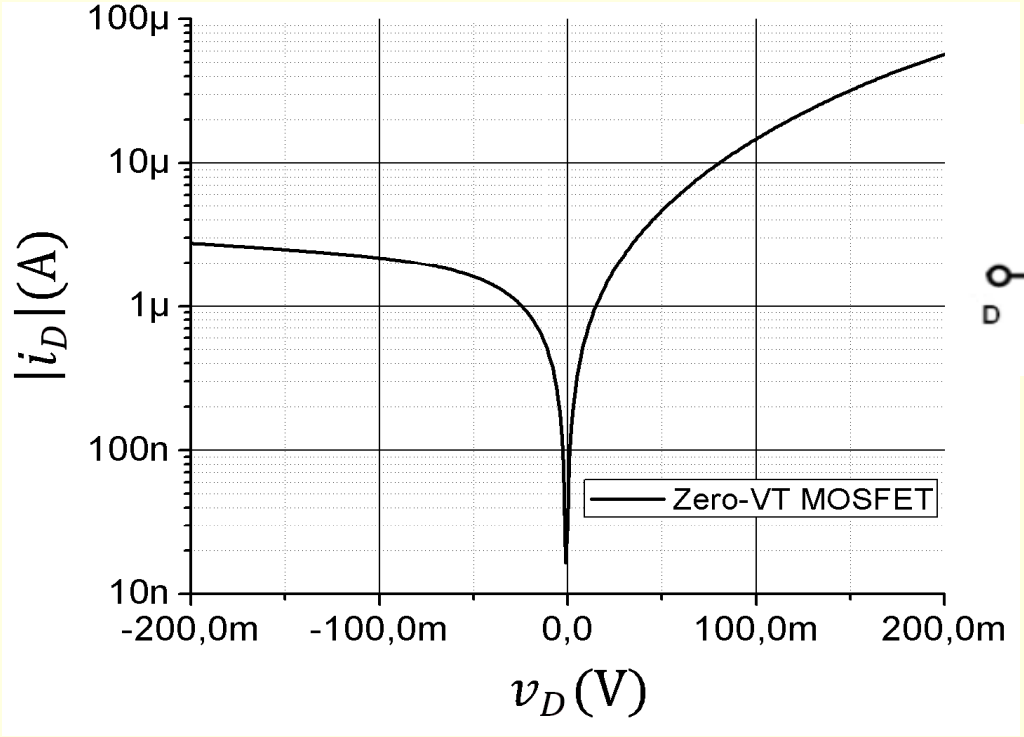
$$V_L = nV_{CI}$$

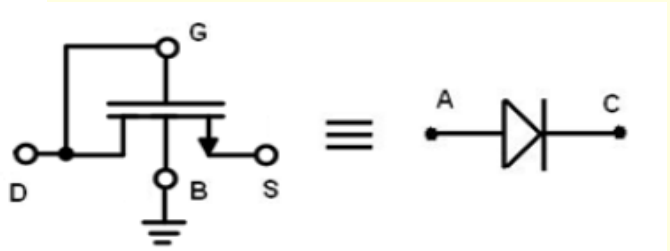
N-stage voltage multiplier

Applications:

- **Generation of voltages higher than the supply voltage, for EEPROMs, flash memories**
- **Energy harvesting for RFID tag chips, for example**

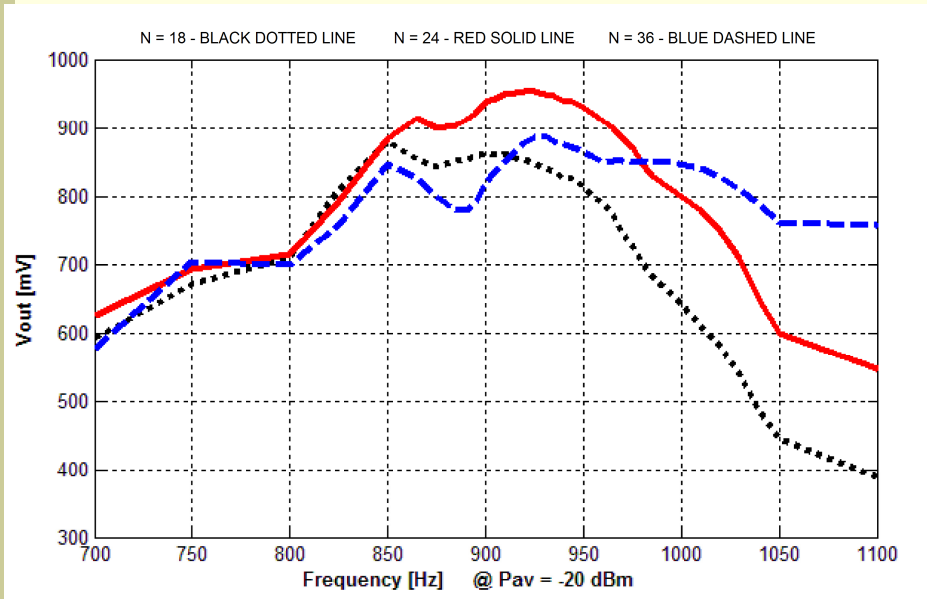
Diode connected MOSFET

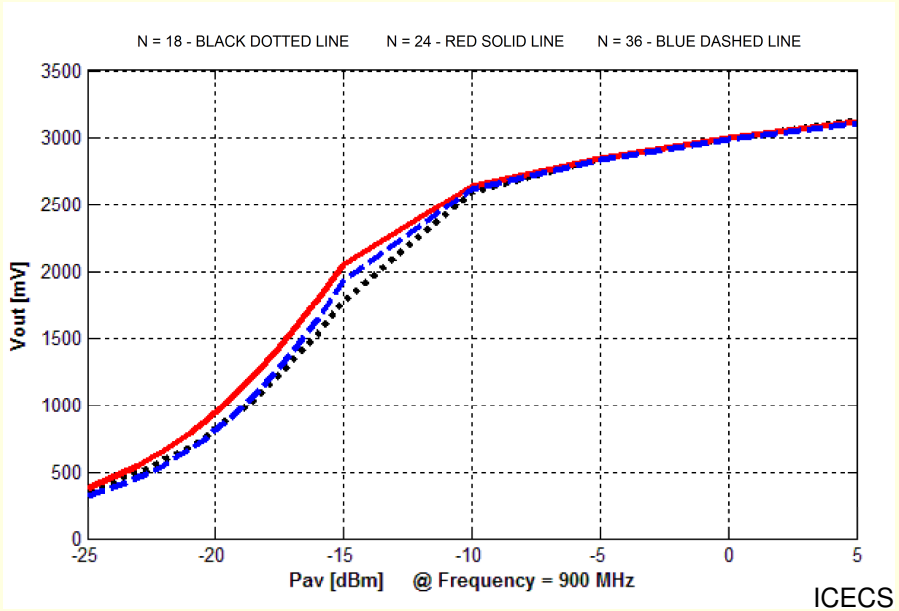


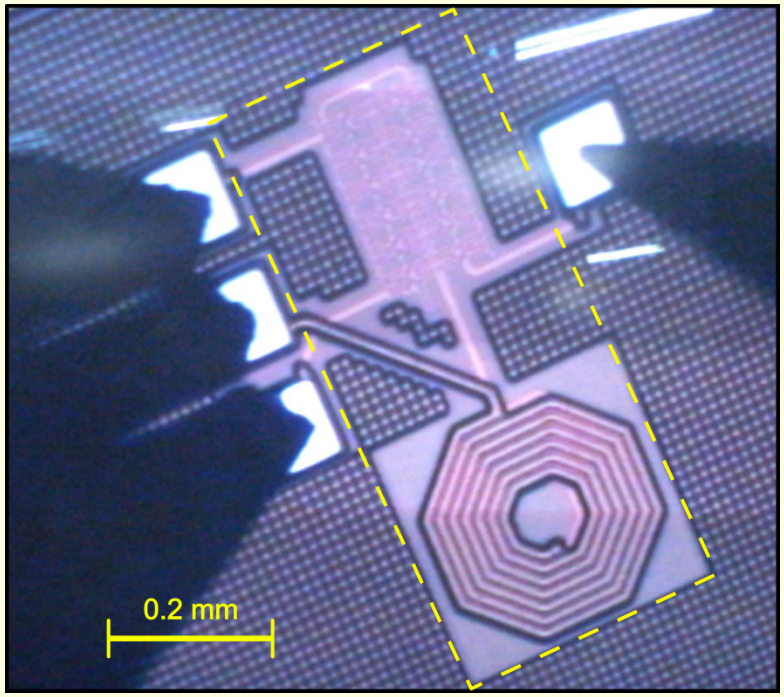


Low-voltage I-V characteristic of a diode-connected zero-VT transistor.

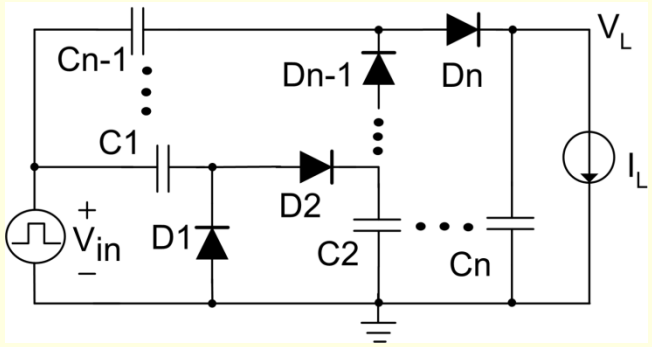
AC/DC converter in 130 nm CMOS technology







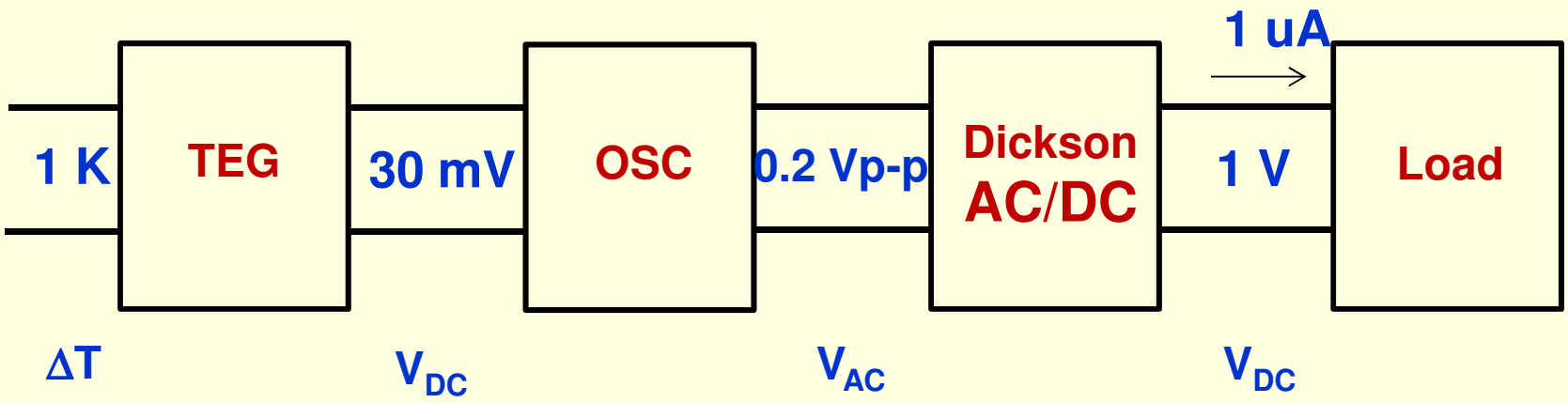
24-stage rectifier



ULTRA-LOW-VOLTAGE (ULV) IC DESIGN: DESIGNING FOR VDD BELOW kT/q

Chapter 4
Ultra-Low-Voltage (ULV) oscillators

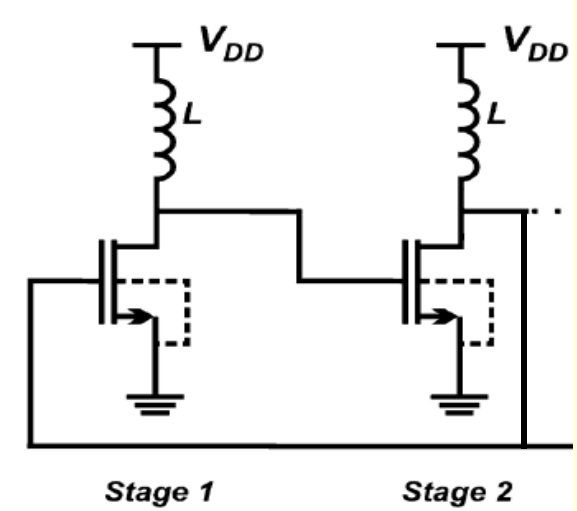
An important application of ULV oscillators



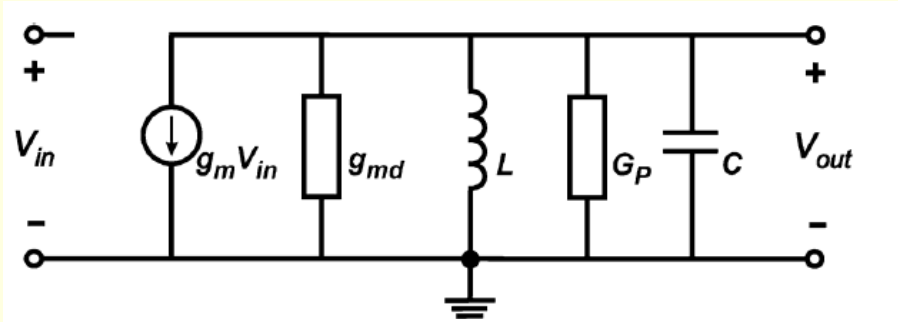
TEG – thermoelectric generator

OSC – oscillator

Inductive ring oscillator - 1



Cross-coupled LC oscillator



$$\frac{V_{out}}{V_{in}} = -\frac{g_m}{g_{md}+G_P}\frac{1}{1-j\tan\phi}$$

$$\tan\phi = \frac{1-LC\omega^2}{\omega L(g_{md}+G_p)}$$

Criterion for oscillation (Barkhausen)

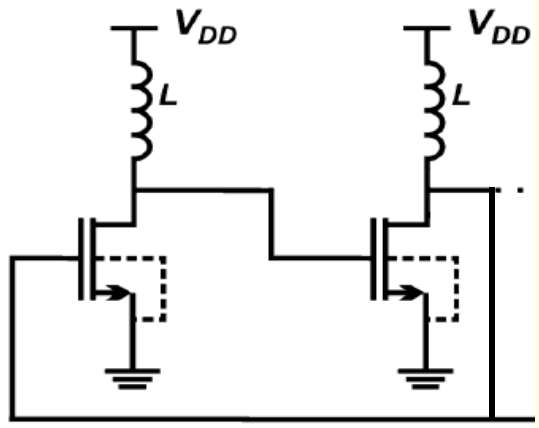
$\phi=0$ & $V_{out}/V_{in}=-1$

$$\omega^2 LC = 1$$

$$\frac{g_m}{g_{md}+G_P} = 1$$

What´s the minimum V_{DD} for oscillation?

Inductive ring oscillator - 2



Cross-coupled LC oscillator

Oscillation frequency $\omega^2 LC = 1$

Voltage gain $\dfrac{g_m}{g_{md} + G_P} = 1$

What´s the minimum V_{DD} for oscillation?

Recall that $g_m = \dfrac{g_{ms} - g_{md}}{n}$

Voltage gain=1 ⟹ (i) $\dfrac{g_{ms}}{g_{md}} = 1 + n\left(1 + \dfrac{G_P}{g_{md}}\right)$

In weak inversion ⟹ (ii) $\dfrac{g_{ms}}{g_{md}} = e^{V_{DS}/\varphi_t} = e^{V_{DD}/\varphi_t}$ since $V_G = V_D = V_{DD}$

$$V_{DD,\min} = \varphi_t \ln\left[1 + n\left(1 + \frac{G_P}{g_{md}}\right)\right] = \varphi_t \ln[1+n] \quad \text{for} \quad \frac{G_P}{g_{md}} << 1$$

Similar to the result (/2) of the CMOS inverter

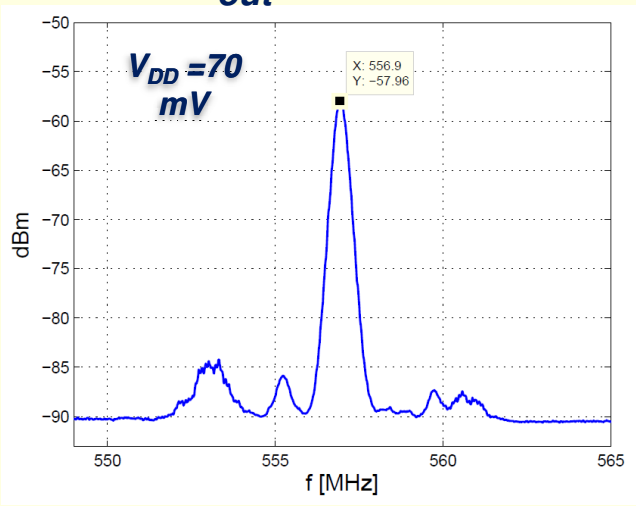
Inductive ring oscillator - 3

7-stage ring oscillator

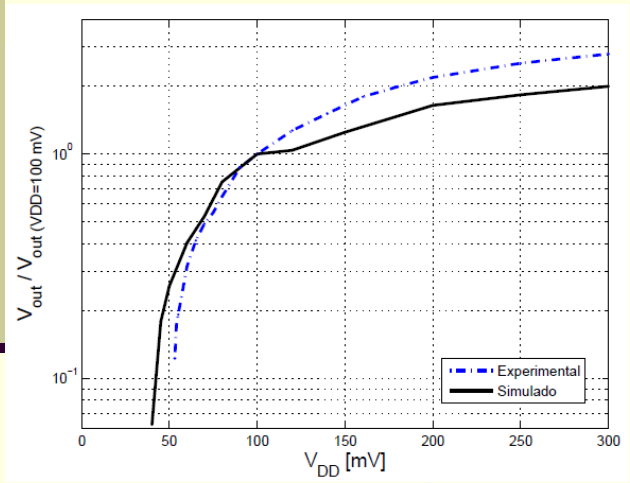
Zero-VT
W/L = 150 µm / 0.48 µm

L_{nom}=100 nH

V_{out} x f

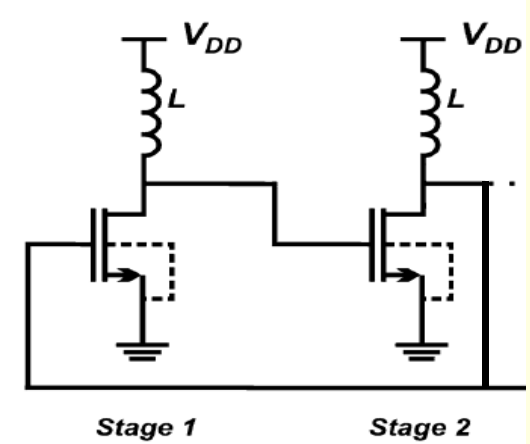


$V_{out\ normalized}$ x V_{DD}



	Calculated	Sch. Sim.	Poslayout	Exp.
VDD,min	32.6 mV	37 mV	40 mV	53 mV
frequency	1.07 GHz	730 MHz	560 MHz	560 MHz

Inductive ring oscillator - 4



Questions:

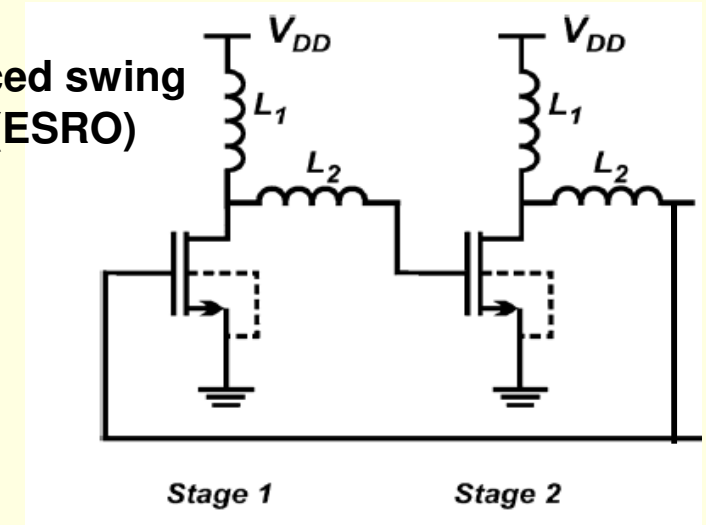
1. How to reduce $V_{DD,min}$?

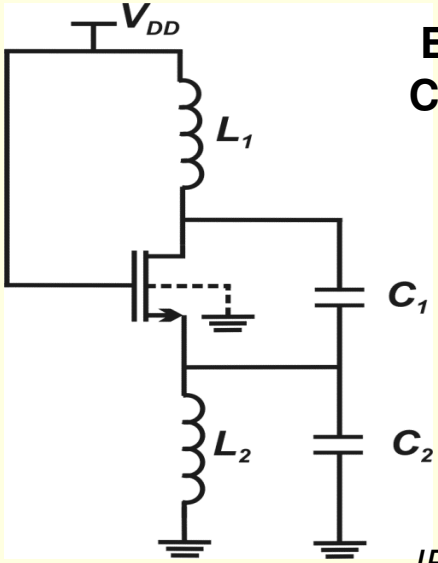
2. How to increase the V_{DD}-limited voltage swing?

Introduce voltage gain from drain to gate

Change topology, e. g., take advantage of CG gain

Enhanced swing IRO (ESRO)

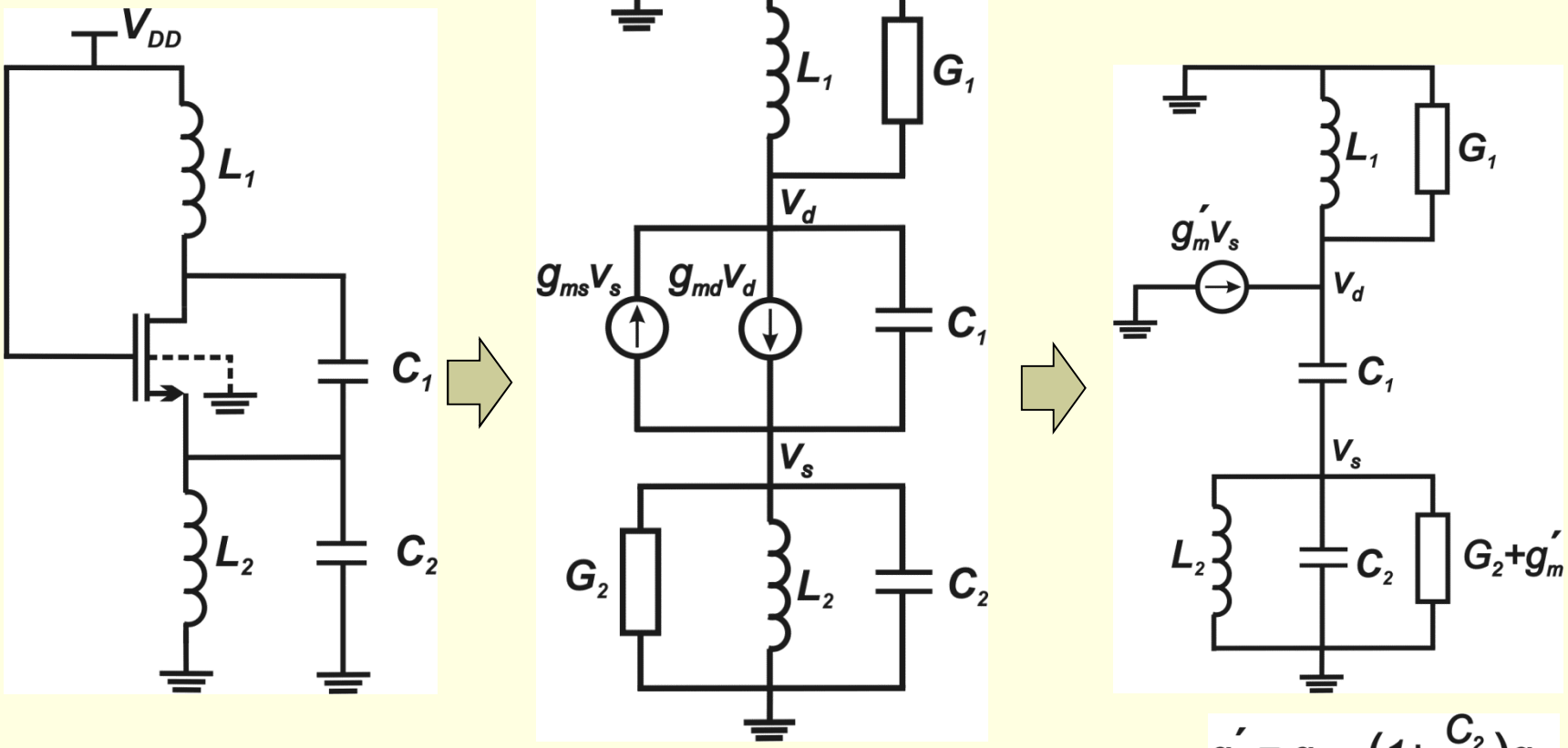




Enhanced swing Colpitts oscillator (ESCO) *

* T. W. Brown et al, *IEEE JSSC*, Aug. 2011.

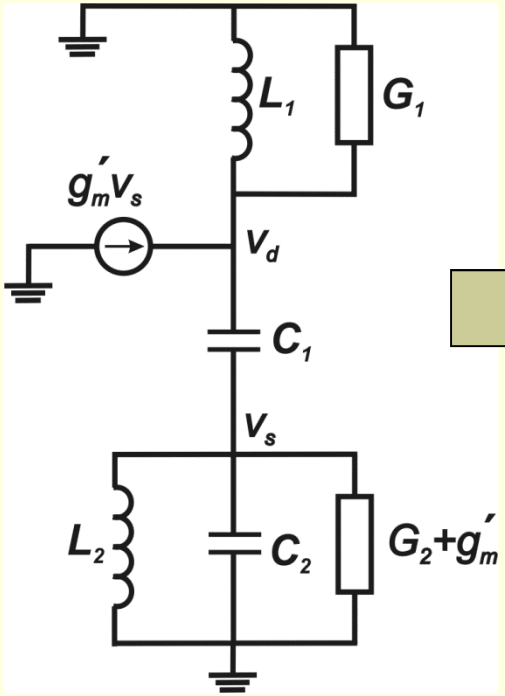
ESCO: small-signal model - 1

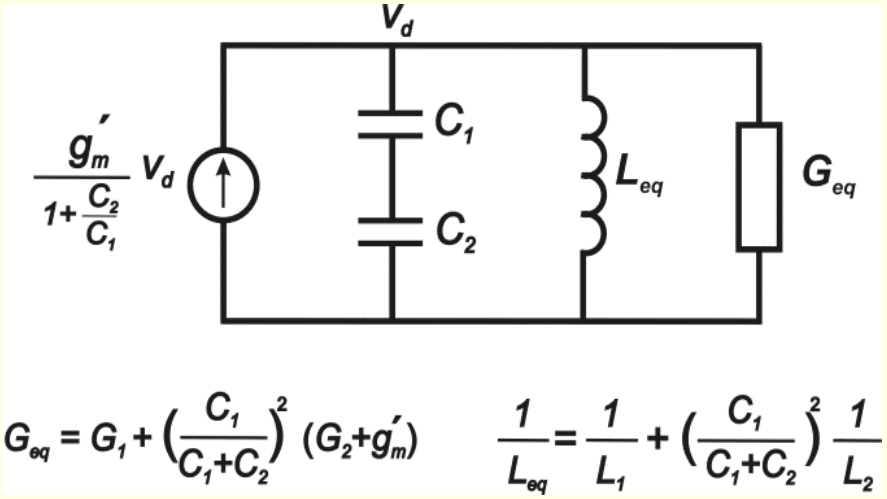


$$g'_m = g_{ms} - \left(1 + \frac{C_2}{C_1}\right) g_{md}$$

$$v_s \cong \frac{v_d}{1 + \frac{C_2}{C_1}} \rightarrow g_{ms} v_s - g_{md} v_d \cong g'_m v_s$$

ESCO: small-signal model - 2

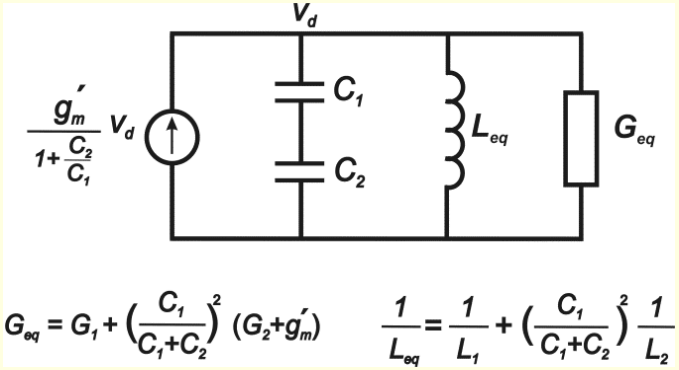




Second-order small-signal model of the ES Colpitts oscillator.

ESCO: start-up condition

$$g_{ms} > \left(1+\frac{C_2}{C_1}\right) g_{md} + \frac{C_1}{C_2} G_2 + \left(2+\frac{C_1}{C_2}+\frac{C_2}{C_1}\right) G_1$$



Optimum value of capacitors to minimize g_{ms} (for the conventional Colpitts $g_{md} = G_2 = 0$!)

$$\frac{C_2}{C_1} = \sqrt{\frac{G_1+G_2}{g_{md}+G_1}}$$

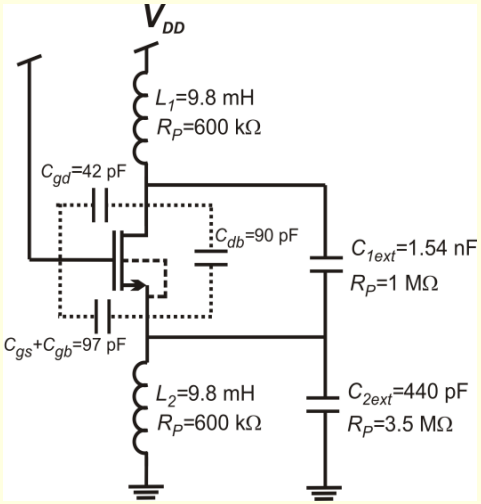
For ideal inductors (and capacitors) $G_1 = G_2 = 0$

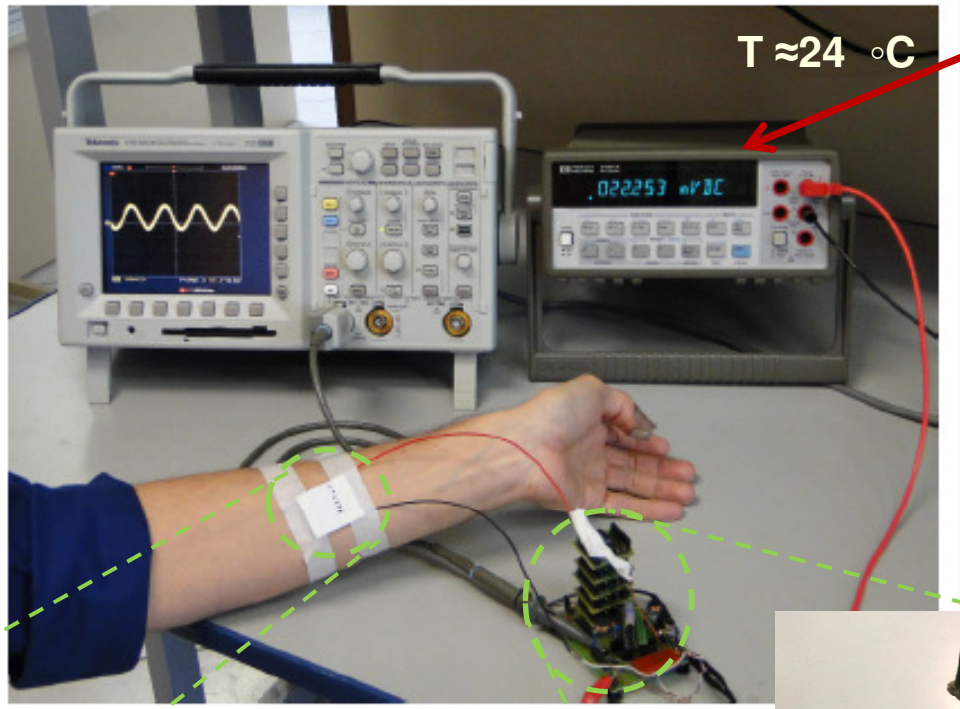
$$g_{ms} > \left(1+\frac{C_2}{C_1}\right) g_{md}$$

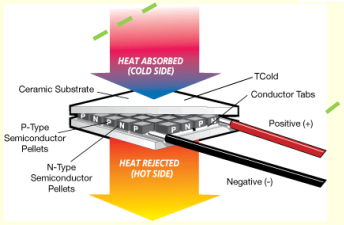
$$V_{DD\,\mathrm{lim}} = \frac{kT}{q} \ln\left(1+\frac{C_2}{C_1}\right)$$

Colpitts oscillator: first prototype

Powered by a thermoelectric generator

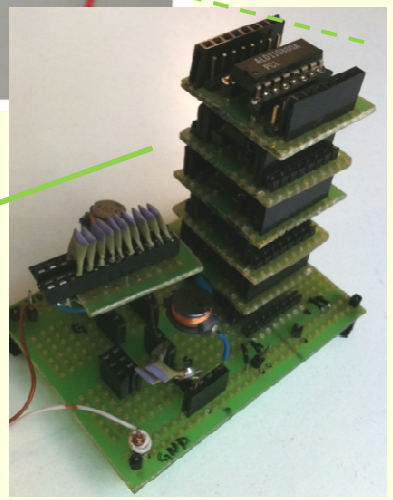






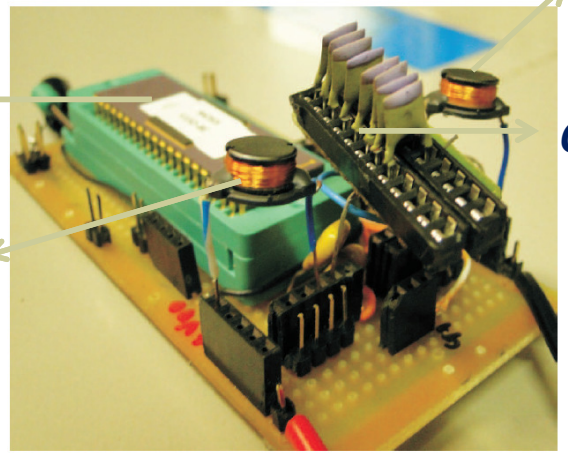
thermoelectric generator

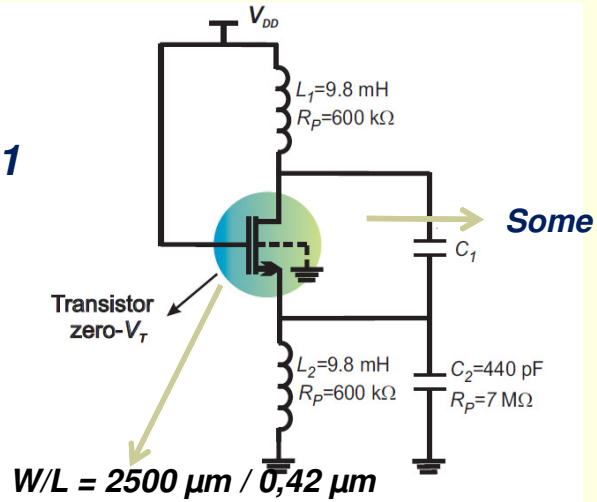
24 // NMOS
Zero-VT (ALD 1108)
VT=59 mV, IS=11.2 uA

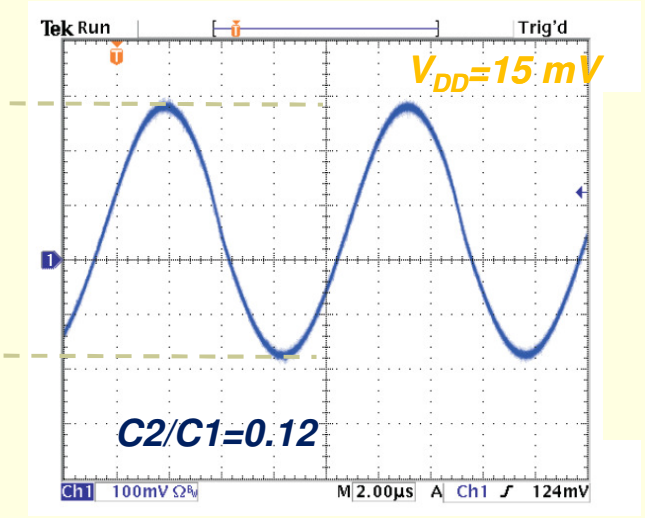


Colpitts oscillator: second prototype

Vdd < 20 mV

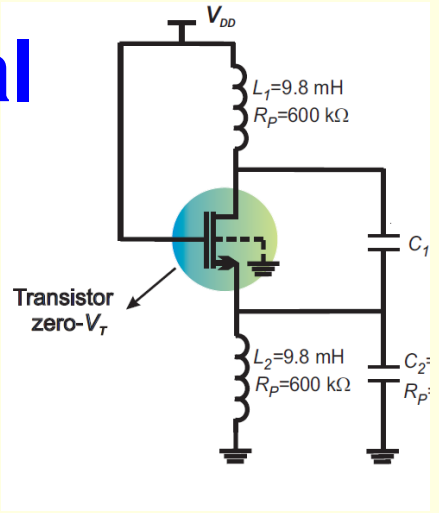




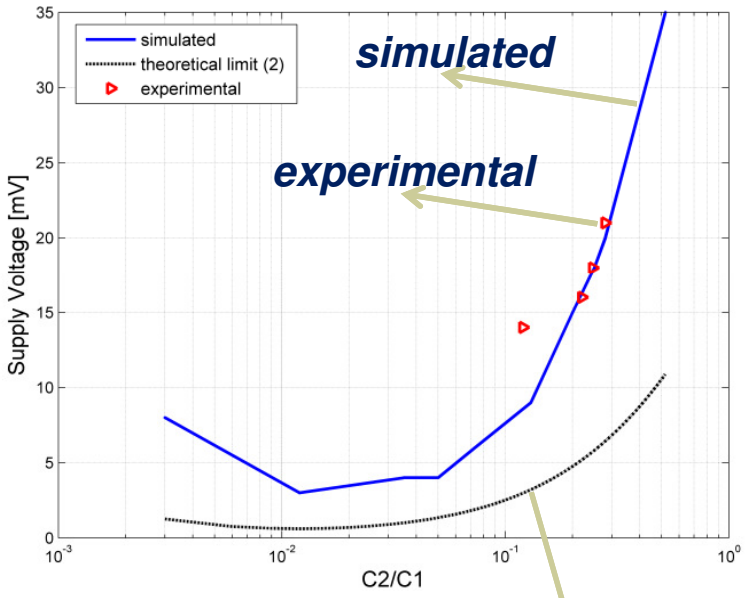


f_{osc}≈110 kHz
V_{DD}=15 mV

Second prototype: experimental results

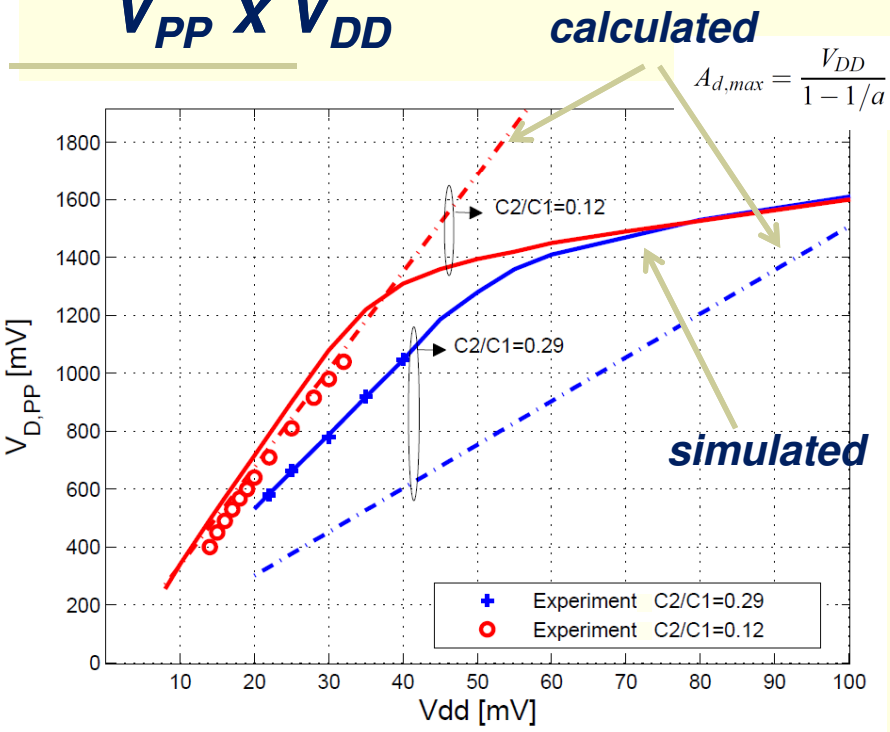


$V_{DD,min}$ x C2/C1

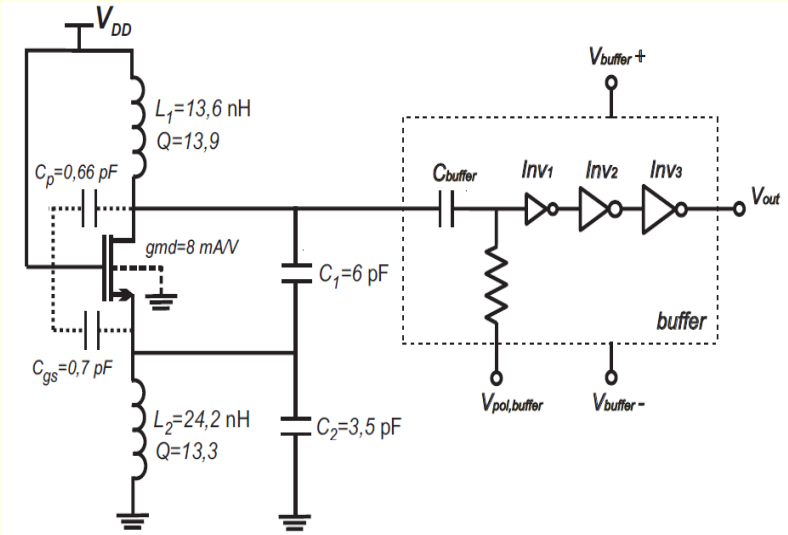


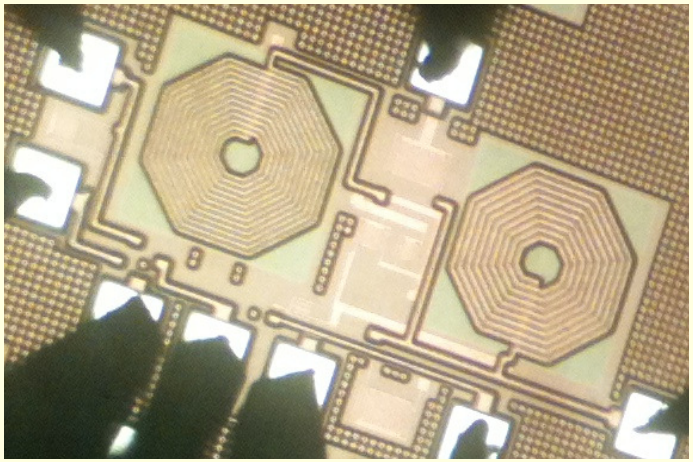
f_{osc}≈110 kHz

V_{PP} x V_{DD}



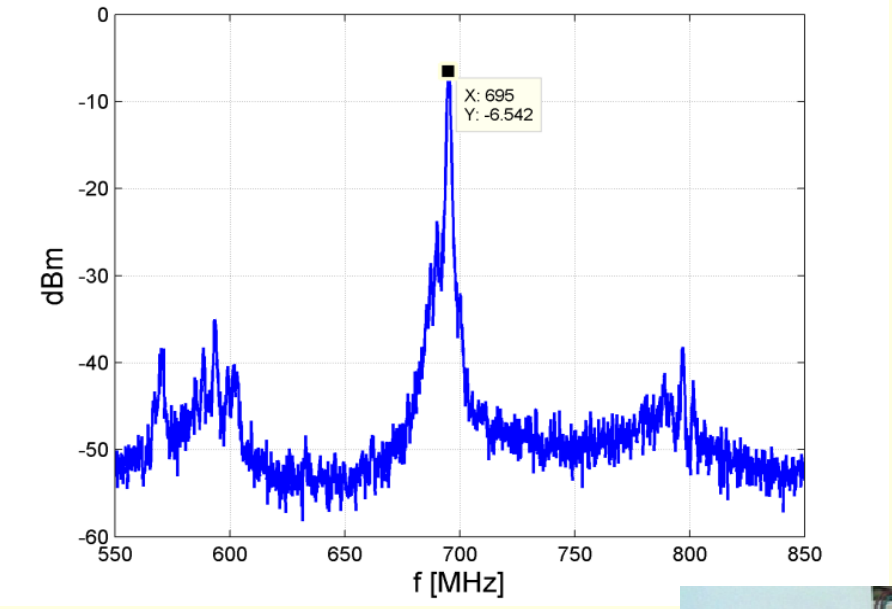
ESCO designed for operation at 800 MHz

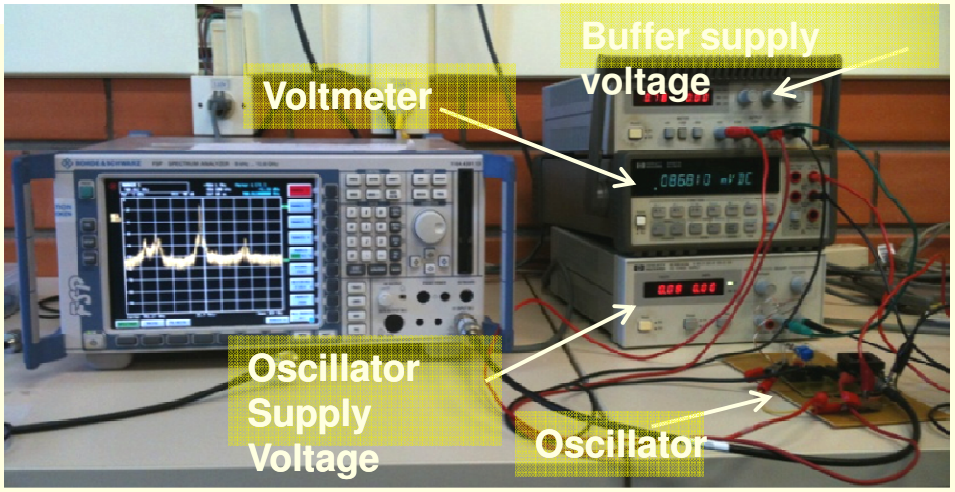




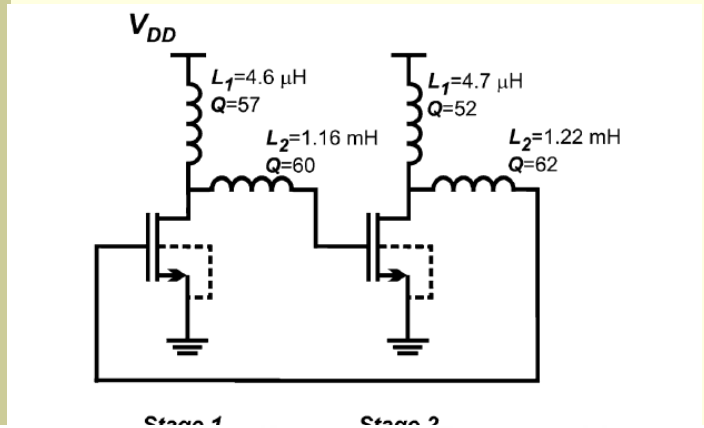
- Micrograph of the ESCO built in 130 nm technology

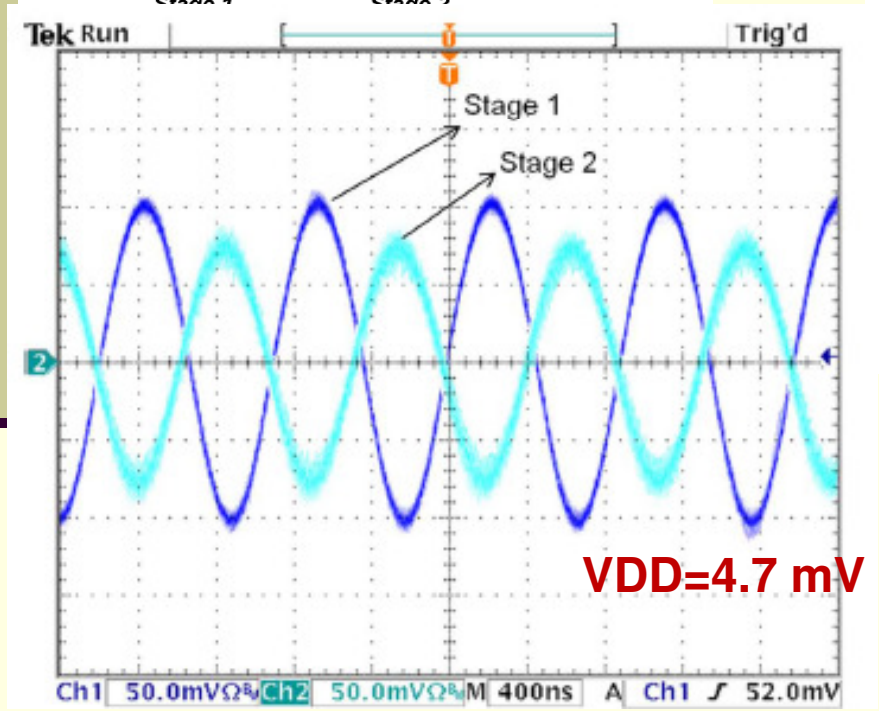
Spectral diagram of the ESCO (V_{DD} = 86 mV)

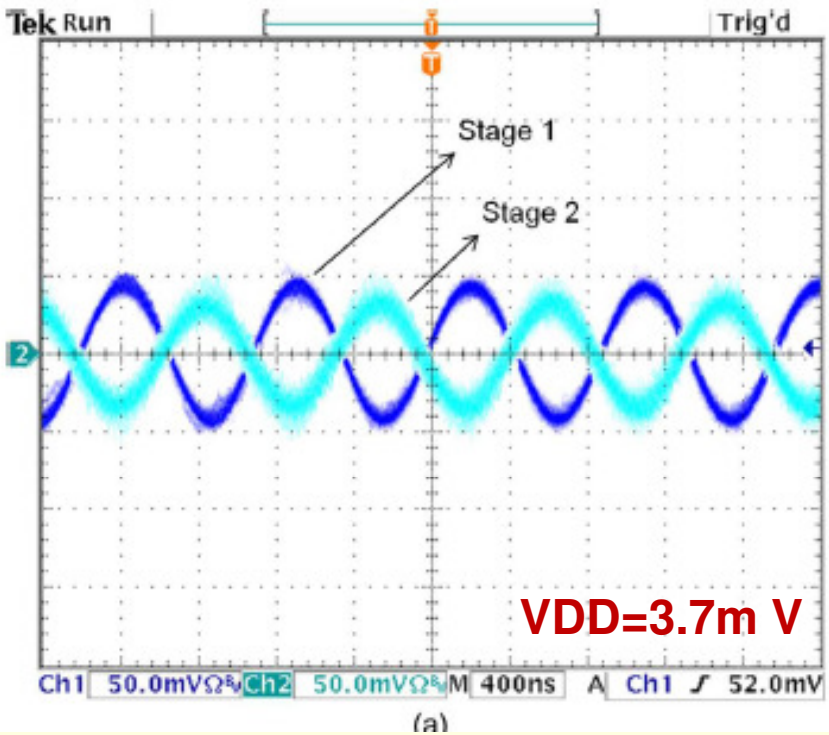




Enhanced swing IRO (ESRO)-1

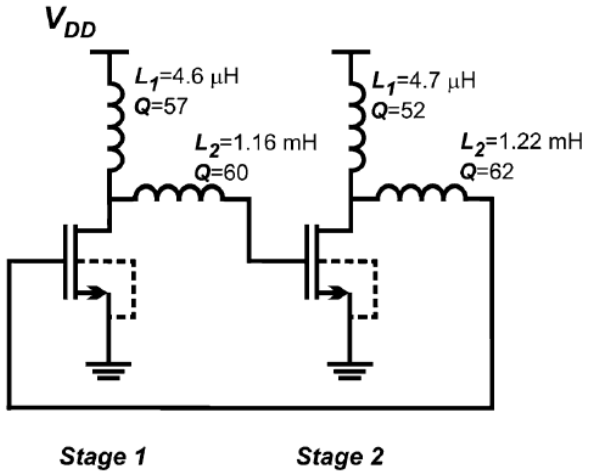






(a)

Enhanced swing IRO (ESRO)-2



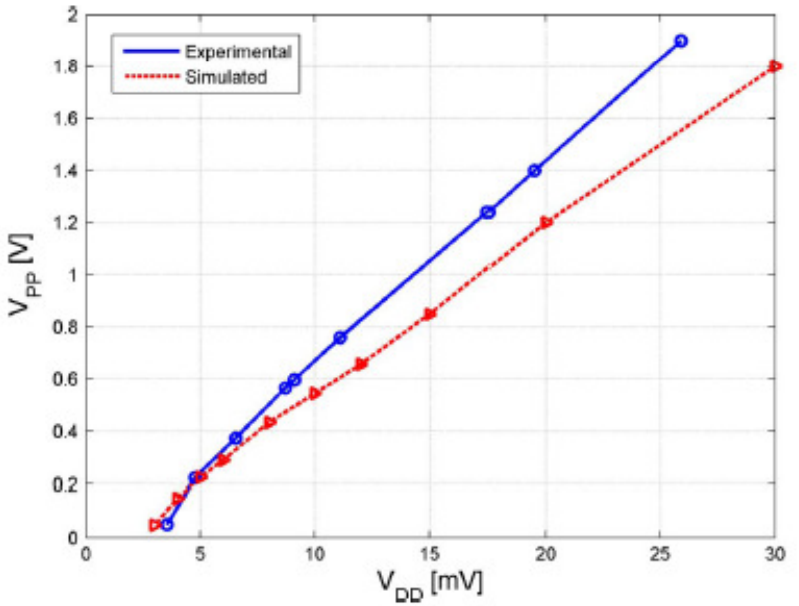


Fig. 12. Simulated (dotted line) and experimental (solid line) peak-to-peak gate voltage versus supply voltage of the ES inductive-load ring oscillator.

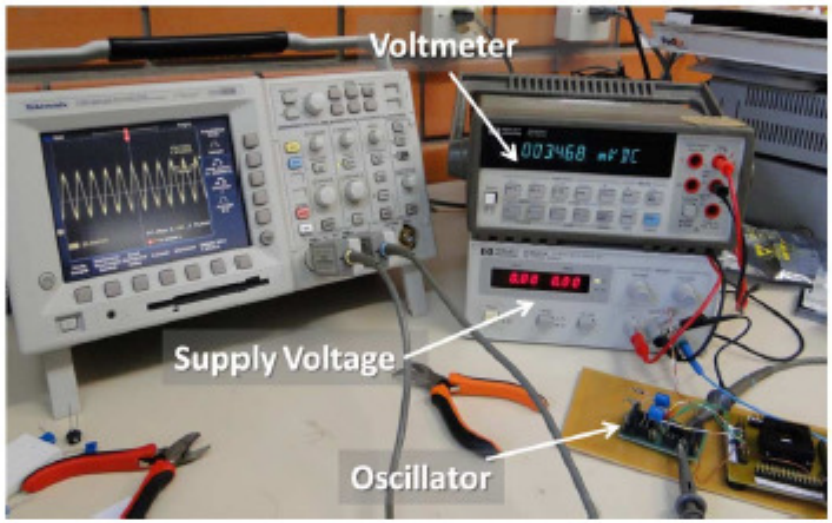


Fig. 13. Picture showing the discrete prototype of the enhanced swing inductive-load oscillator and test equipment.

TABLE I

EXPERIMENTAL RESULTS FOR THE OSCILLATION FREQUENCY AND MINIMUM SUPPLY VOLTAGE OF THE OSCILLATOR TOPOLOGIES

Topology	Theoretical V_{dd} (min) *	IC prototype 130nm CMOS		Discrete prototype	
		V_{dd} (min)	f_{osc}	V_{dd} (min)	f_{osc}
ILRO	$\phi_t \ln(1+n)$	53 mV	550 MHz	50 mV	11 MHz
ESILRO	$\phi_t \ln\left(1+n\frac{L_1}{L_1+L_2}\right)$	30 mV+	400 MHz	3.5 mV	1.1 MHz
ESCO	$\phi_t \ln\left(1+\frac{C_2/C_1}{1+L_1/L_2}\right)$	86 mV	700 MHz	15 mV	108 kHz

* For lossless passive devices and operation of MOSFETs in weak inversion

\+ Post-layout simulation

ILRO, ESILRO, and ESCO refer to inductive-load ring, enhanced swing inductive-load ring, and enhanced swing Colpitts oscillators, respectively.

Values of components:

ILRO – IC prototype – L = 100 nH, Q = 8.

ILRO – discrete prototype – L = 4.6 uH, Q = 50.

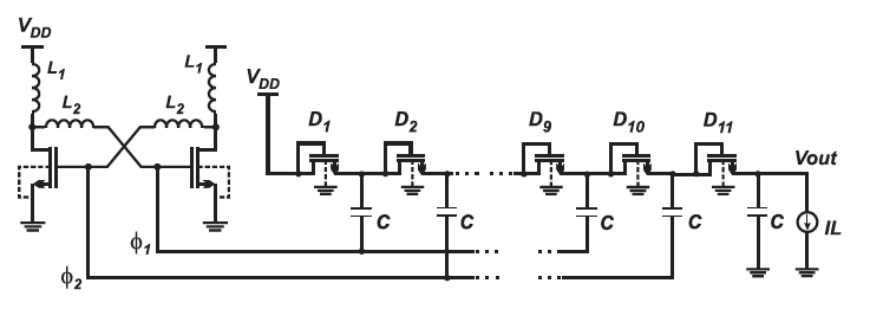
ESILRO – IC prototype – L_1 = 20 nH, Q_1 = 9; L_1 = 80 nH, Q_2 = 8.

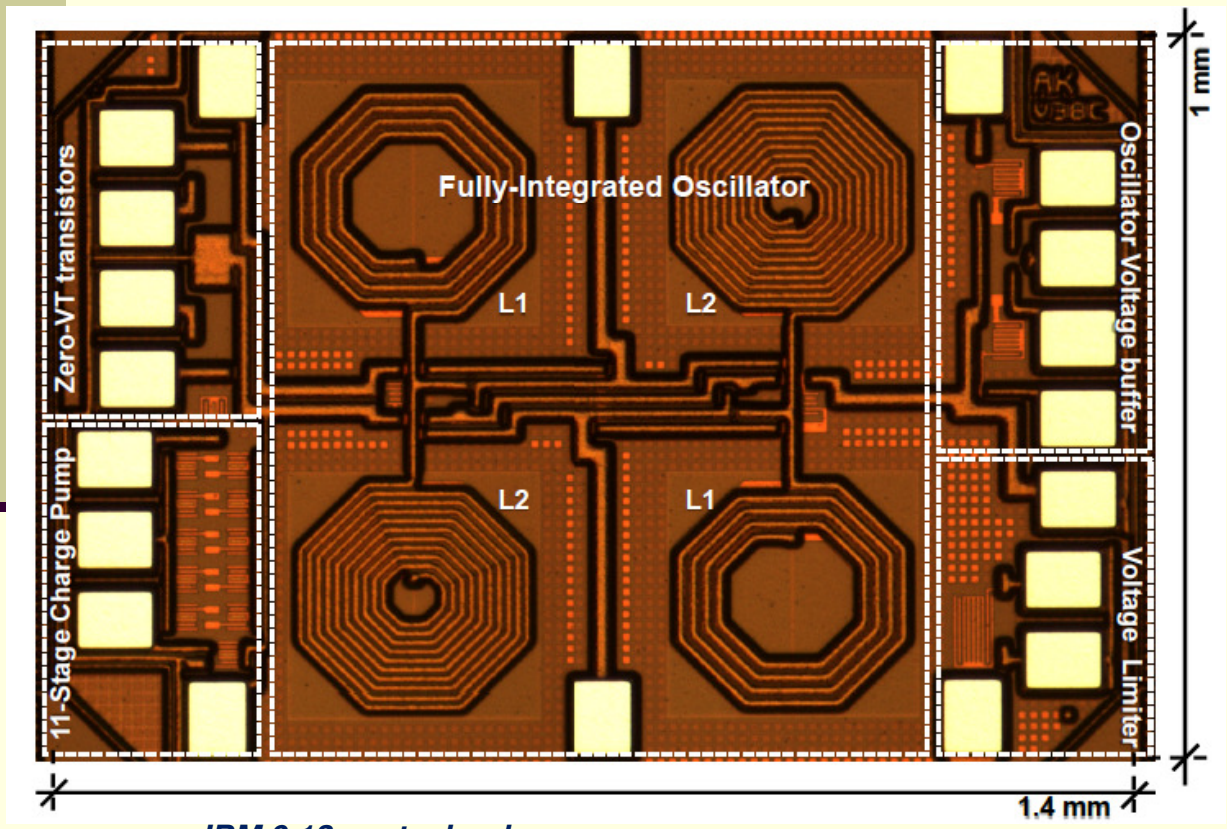
ESILRO – discrete prototype – L_1 = 4.6 uH, Q_1 = 55, L_2 = 1.2 mH, Q_2 = 60.

ESCO – IC prototype – L_1 = 13.6 nH, Q_1 = 13.9, L_2 = 24.2 nH, Q_2 = 13.3, C_1 = 6 pF, C_2 = 3.5 pF.

ESCO – discrete prototype – $L_1 = L_2$ = 9.8 mH, $Q_1 = Q_2$ = 80, C_1 = 1.54 nF, C_2 = 0.44 nF.

Step-up converter-1





IBM 0.13 µm technology

11-stage Dickson charge pump

Zero-VT transistor as a diode
W/L=4.2µm/0.42µm
V_T=76.5 mV
Isat = 500 nA

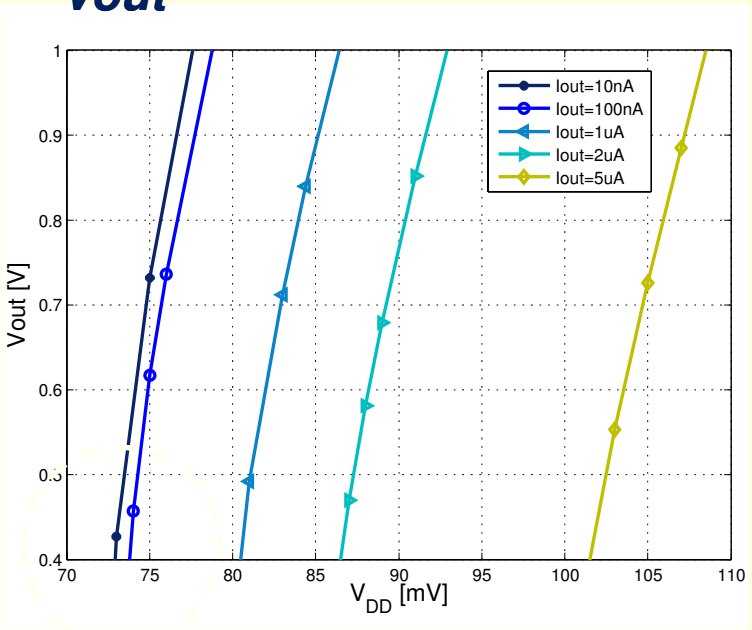
2-stage ESRO

Zero-VT transistor
W/L=500µm/0.42µm
V_T=63 mV
Integrated inductors
L_1=18.8 nH, L_2= 66 nH
Q ≈ 8

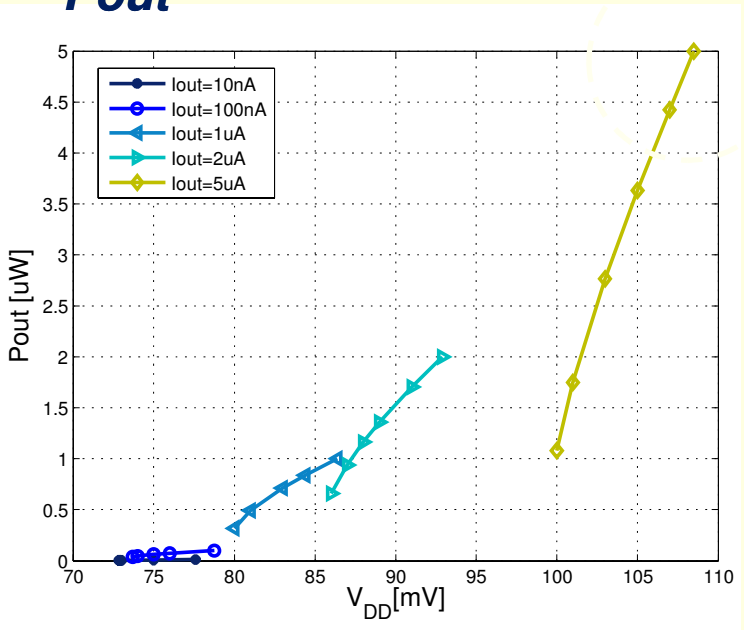
Step-up converter-2

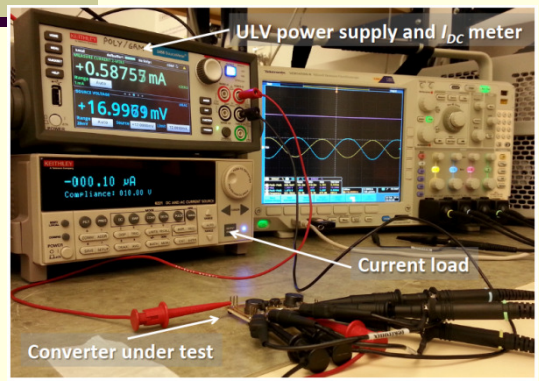
Experimental results

Vout



Pout





Start-up

$V_{DD,min}$ = 73 mV

at V_{out} *= 1 V*
I_L *= 1 uA*

V_{DD} = 86 mV

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